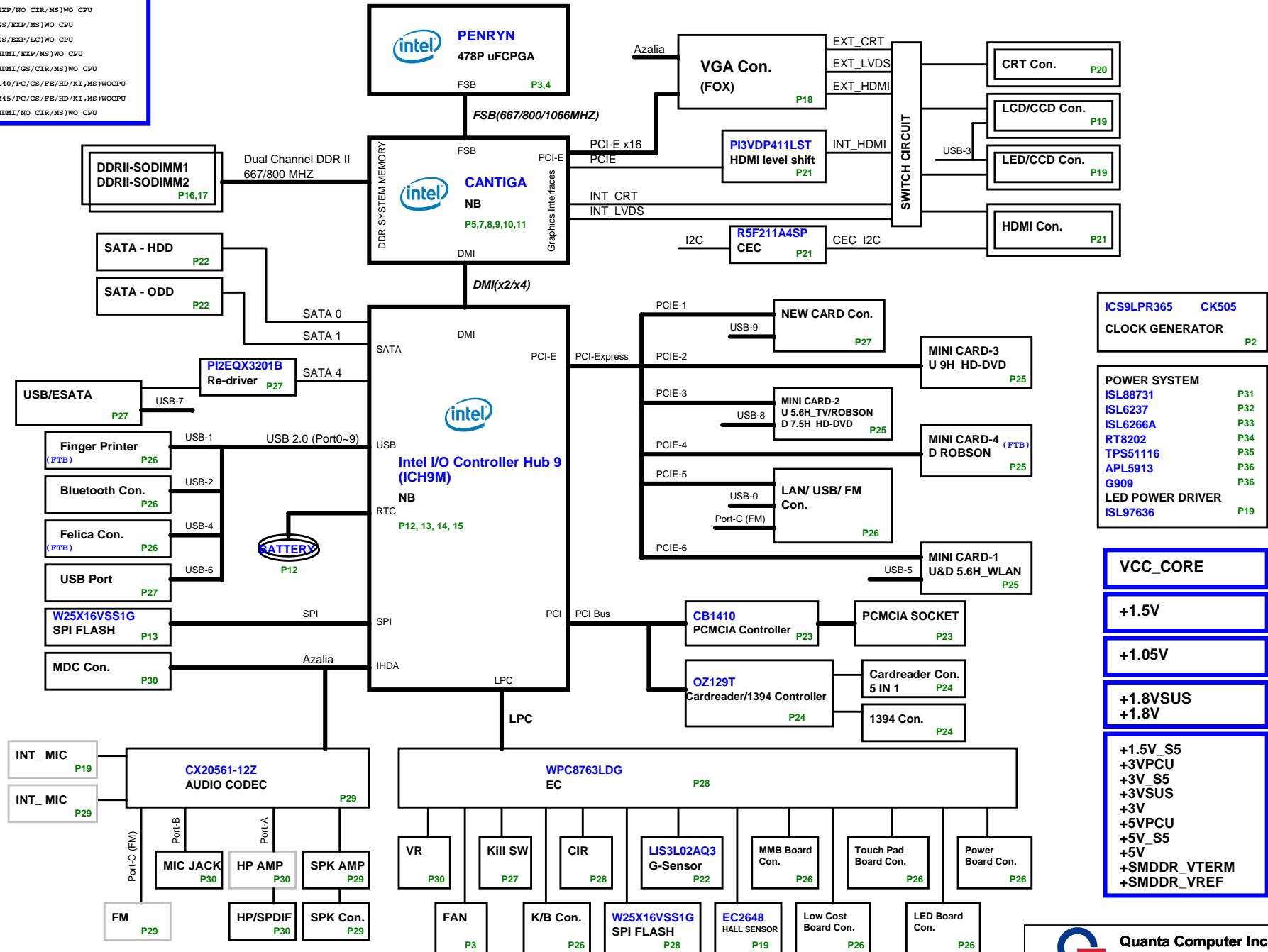


VER : E3D

BOM P/N	Description
31TE1MB0010	TE1M MB(PM45/RB/MS)WO CPU
31TE1MB0120	TE1M MB(PM45/MAIN/RB/HDMI/CIR)WO CPU
31TE1MB0130	TE1M MB(GM45/EXP/NO CIR/MS)WO CPU
31TE1MB0140	TE1M MB(GM45/GS/EXP/MS)WO CPU
31TE1MB0170	TE1M MB(GM45/GS/EXP/LC)WO CPU
31TE1MB01N0	TE1M MB(GM45/HDMI/EXP/MS)WO CPU
31TE1MB01M0	TE1M MB(GM45/HDMI/GS/CIR/MS)WO CPU
31TE1MB01P0	TE1M MB ASY(GL40/PC/GS/FB/HD/KI,MS)WOCPU
31TE1MB01Q0	TE1M MB ASY(GM45/PC/GS/FB/HD/KI,MS)WOCPU
31TE1MB01S0	TE1M MB(PM45/HDMI/NO CIR/MS)WO CPU

TE1M Block Diagram



PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : GND1
- LAYER 3 : IN1
- LAYER 4 : VCC
- LAYER 5 : IN2
- LAYER 6 : IN3
- LAYER 7 : GND2
- LAYER 8 : BOT

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA

ICS9LPR365 CK505
CLOCK GENERATOR P2

POWER SYSTEM

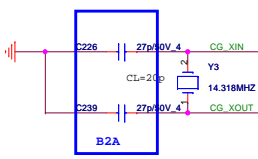
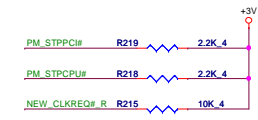
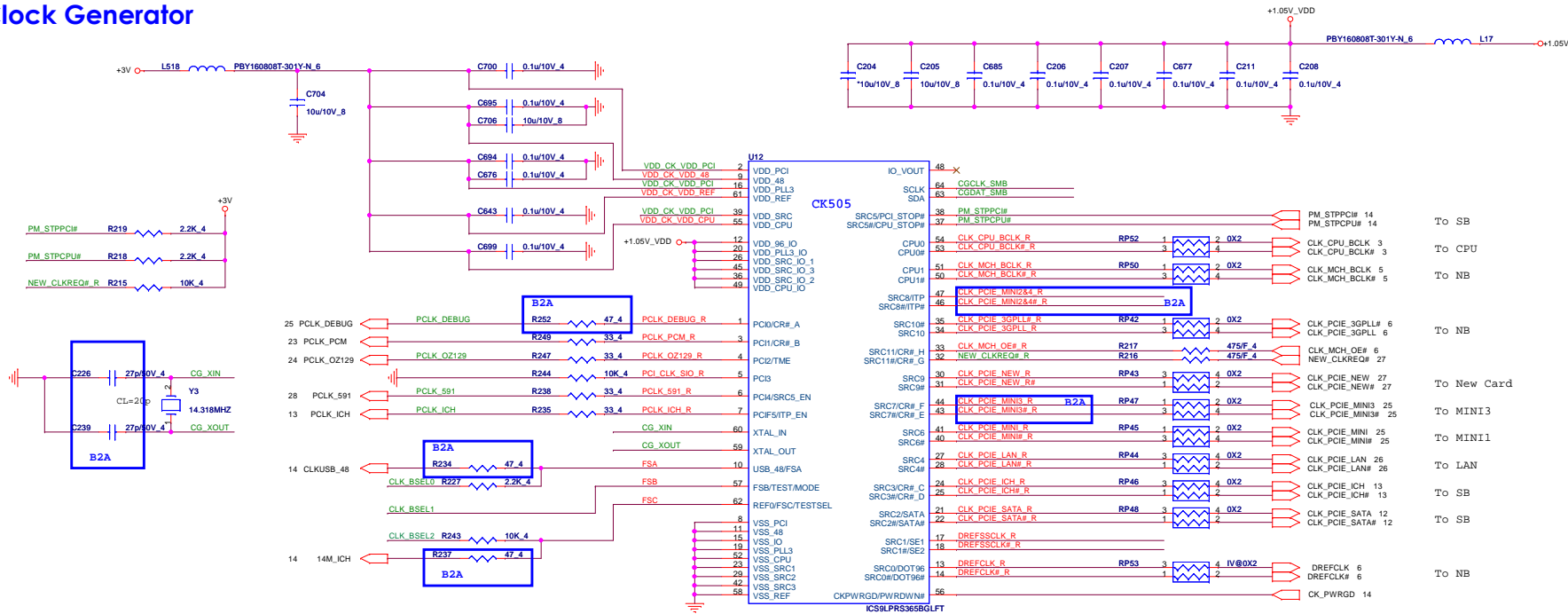
- ISL88731 P31
- ISL6237 P32
- ISL6266A P33
- RT8202 P34
- TPS51116 P35
- APL5913 P36
- G909 P36
- LED POWER DRIVER P19
- ISL97636 P19

VCC_CORE

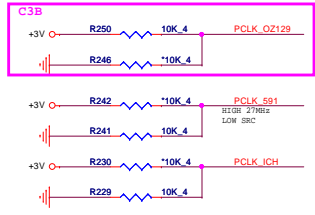
- +1.5V
- +1.05V
- +1.8VSUS
- +1.8V
- +1.5V_S5
- +3VPCU
- +3V_S5
- +3VSUS
- +3V
- +5VPCU
- +5V_S5
- +5V
- +SMDDR_VTERM
- +SMDDR_VREF

Clock Generator

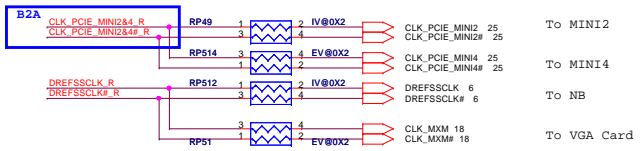
BOM Option Table		
Reference	Description	
IV@	INT VGA	
EV@	EXT VGA	



Pin	Function	Internal PD	NO OVERCLOCKING	(default)	NORMAL RUN
Pin 4	PCI2/TME	Internal PD			
Pin 5	PCI-3	Internal PD	PIR37/38 IS SRC5		PCI_STOP/CPU_STOP (default)
Pin 6	PCI-4/27M_SEL	Internal PD	PIR 17/18 IS 27MHz		IS SRC/DOT (default)
Pin 7	PCI-F/ITP_EN	Internal PD	PIR 46/47 IS CPUITP		PIR 46/47 IS SRC8 (default)



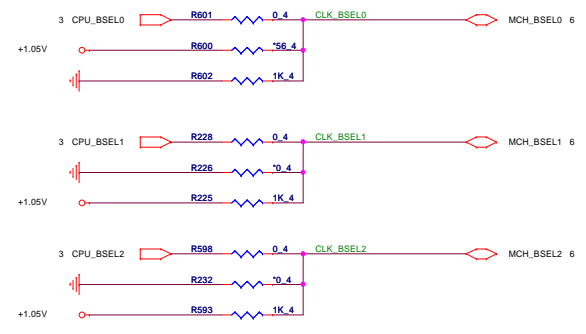
<MAIN>-ICS9LPRS365BGLFT QCI:ALPRS365K13
 <SECOND>-SLG8SP12TTR: QCI:AL8SP12K05



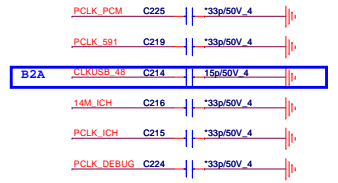
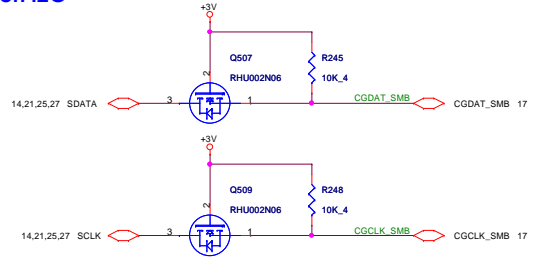
FREQ. SEL TABLE

BSEL Frequency Select Table

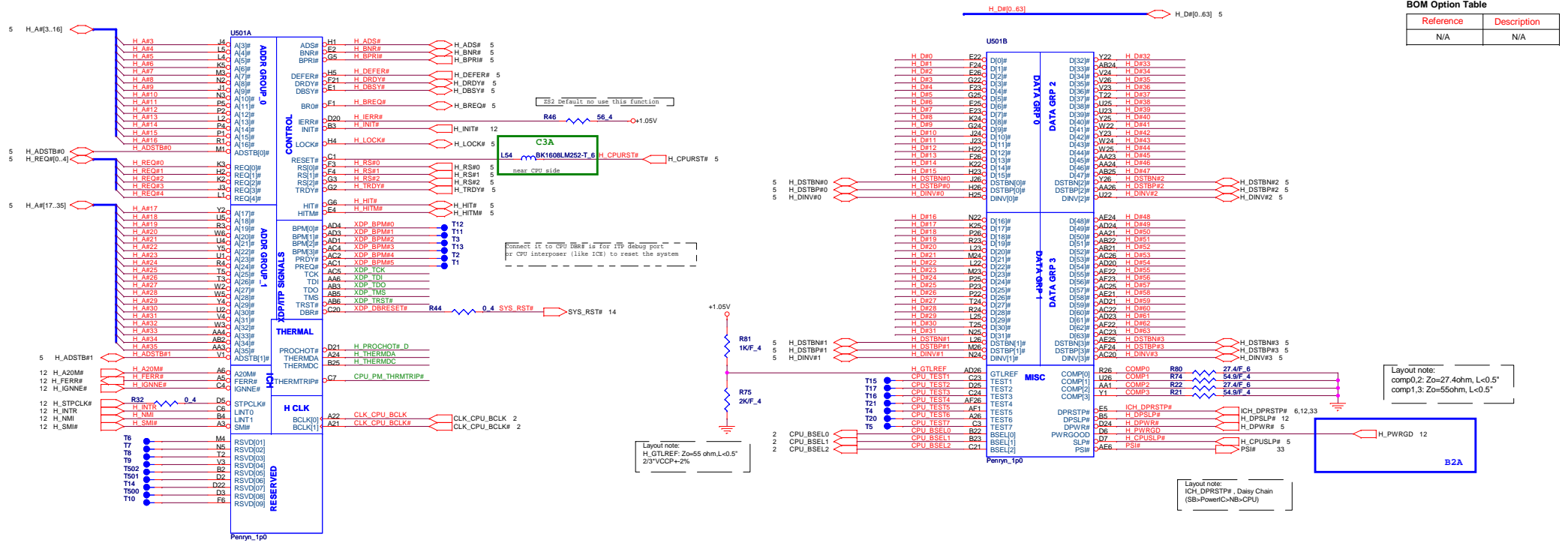
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



Clock Gen I2C

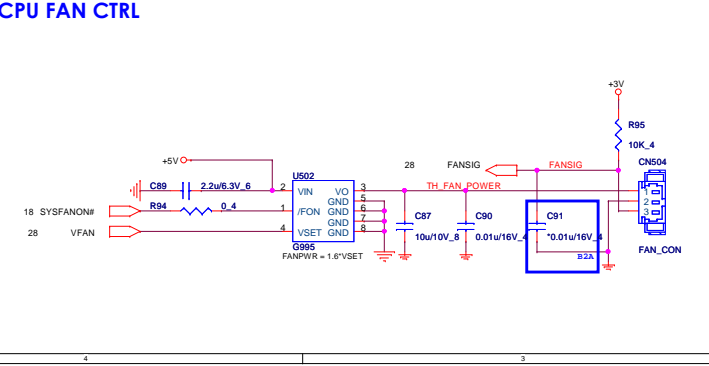
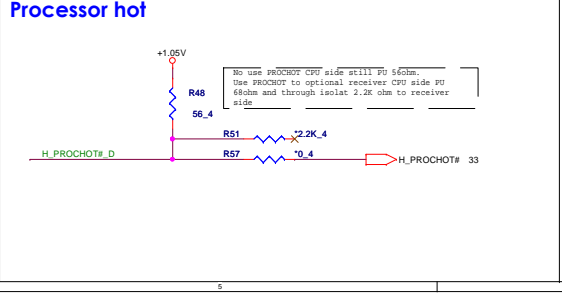
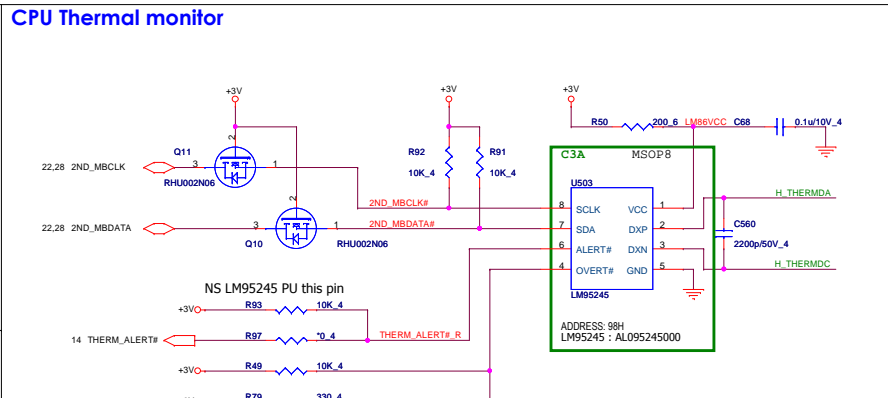
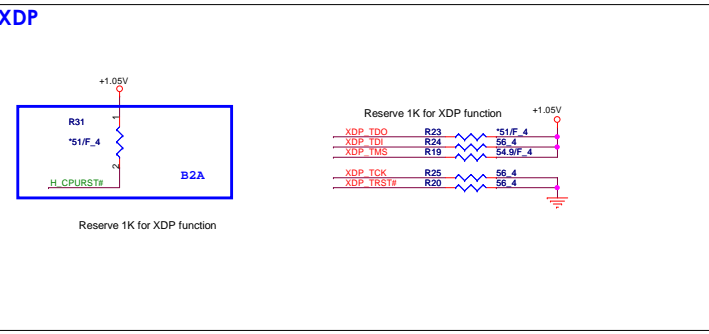
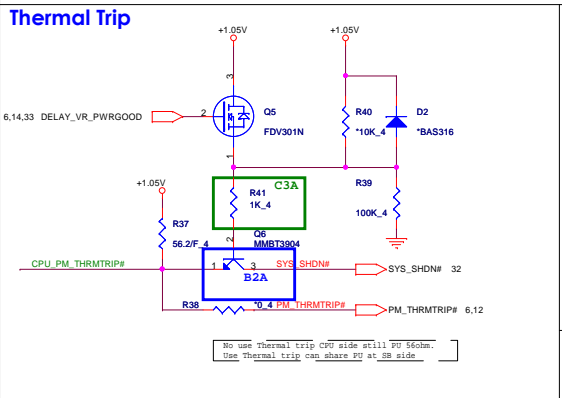


Reference	Description
N/A	N/A



Layout note:
comp0,2: Zo=27.4ohm, L<0.5"
comp1,3: Zo=55ohm, L<0.5"

Layout note:
ICH_DPRSTP#, Daisy Chain
(SB=PowerC>NB>CPU)



Quanta Computer Inc.
PROJECT : TELM

Size: Document Number: CPU(1/2)- Host Bus Rev: E3D
Date: Monday, May 26, 2008 Sheet: 3 of 40

BOM Option Table

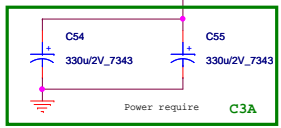
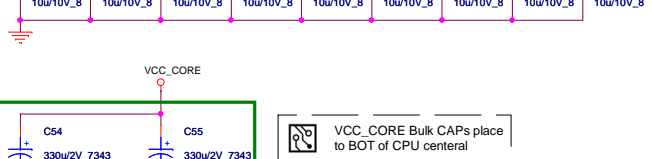
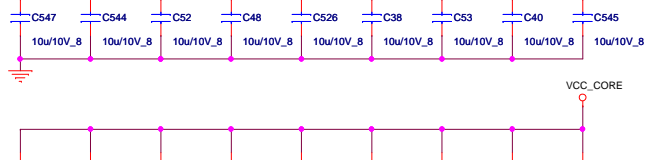
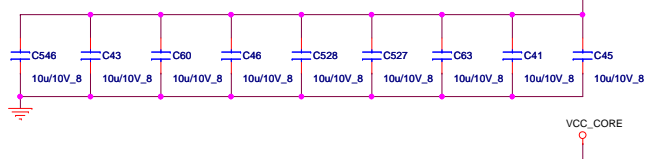
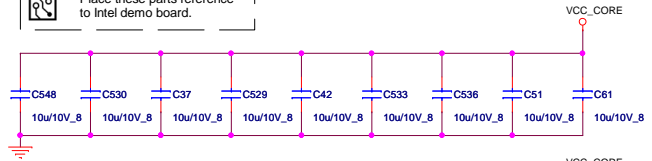
Reference	Description
N/A	N/A

Need NC 20PCS 10u before A1 BOM released(A0 all stuff)

Place these parts reference to Intel demo board.

Layout Note: Inside CPU center cavity in 2 rows

U501D		
A4	VSS[001]	P6
A8	VSS[002]	P21
A11	VSS[003]	P24
A14	VSS[004]	R2
A16	VSS[005]	R5
A19	VSS[006]	R22
A23	VSS[007]	R25
AF2	VSS[008]	T1
B6	VSS[009]	T4
B8	VSS[010]	T23
B11	VSS[011]	T26
B13	VSS[012]	T6
B16	VSS[013]	U6
B19	VSS[014]	U21
B24	VSS[015]	U24
C5	VSS[016]	V5
C9	VSS[017]	V22
C11	VSS[018]	V25
C14	VSS[019]	W1
C16	VSS[020]	W4
C19	VSS[021]	W23
C2	VSS[022]	W26
C22	VSS[023]	Y2
C25	VSS[024]	Y6
D1	VSS[026]	Y21
D4	VSS[027]	Y24
D8	VSS[028]	AA2
D11	VSS[029]	AA5
D13	VSS[030]	AA8
D19	VSS[031]	AA14
D16	VSS[032]	AA18
D23	VSS[033]	AA16
D26	VSS[034]	AA19
E3	VSS[035]	AA22
E6	VSS[036]	AA25
E8	VSS[037]	AB1
E11	VSS[038]	AB4
E14	VSS[039]	AB8
E16	VSS[040]	AB11
E19	VSS[041]	AB13
E21	VSS[042]	AB19
E24	VSS[043]	AB23
F5	VSS[044]	AC3
F8	VSS[045]	AC6
F11	VSS[046]	AC8
F13	VSS[047]	AC11
F16	VSS[048]	AC14
F19	VSS[049]	AC16
F2	VSS[050]	AC19
F22	VSS[051]	AD1
F25	VSS[052]	AD2
G4	VSS[053]	AD5
G3	VSS[054]	AD8
G26	VSS[055]	AD11
H3	VSS[056]	AD13
H6	VSS[057]	AD16
H21	VSS[058]	AD19
H24	VSS[059]	AD22
J2	VSS[060]	AE1
J5	VSS[061]	AE4
J22	VSS[062]	AE8
J25	VSS[063]	AE11
K1	VSS[064]	AE14
K4	VSS[065]	AE16
K23	VSS[066]	AE19
K26	VSS[067]	AE23
L3	VSS[068]	AE26
L6	VSS[069]	A2
L21	VSS[070]	AF6
L24	VSS[071]	AF8
M2	VSS[072]	AF11
M5	VSS[073]	AF13
M22	VSS[074]	AF16
M25	VSS[075]	AF19
N1	VSS[076]	AF21
N4	VSS[077]	AF25
N11	VSS[078]	
N23	VSS[079]	
N26	VSS[080]	
P3	VSS[081]	
	VSS[082]	
	VSS[083]	
	VSS[084]	
	VSS[085]	
	VSS[086]	
	VSS[087]	
	VSS[088]	
	VSS[089]	
	VSS[090]	
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	VSS[092]	
	VSS[093]	
	VSS[094]	
	VSS[095]	
	VSS[096]	
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	VSS[098]	
	VSS[099]	
	VSS[100]	



VCC_CORE Bulk CAPs place to BOT of CPU central

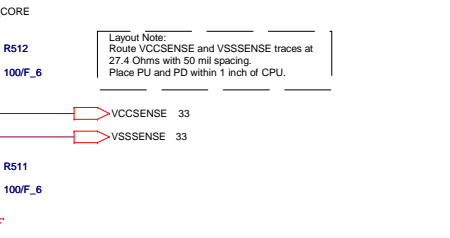
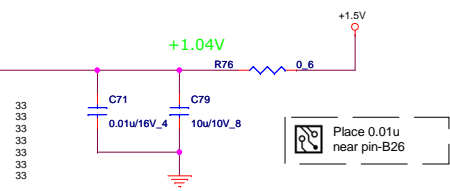
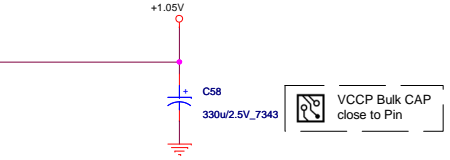
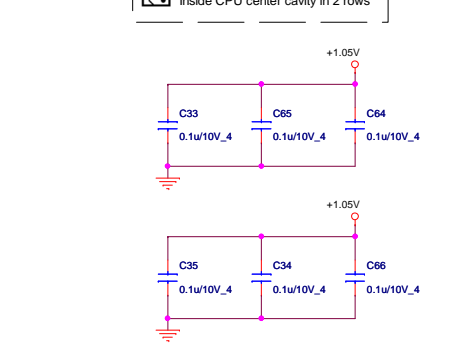
Penryn CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	47A	Standard Voltage CPU
VCC_CORE	O	X	X	VID	50A	SV Design Target
VCC_CORE	O	X	X	VID	TBD	Extreme Edition CPU
VCC_CORE	O	X	X	VID	67A	EE Design Target
VCCA	O	X	X	+1.5V	130mA	
VCCP	O	X	X	+1.05V	4.5A	Before VCC Stable
VCCP	O	X	X	+1.05V	2.5A	After VCC Stable

(See Penryn EMTS Rev:1.0 Table7,8 for voltage and current)

(See Penryn EMTS Rev:1.0 Table-3 for VID table)

U501C		
A7	VCC[001]	VCC[068]
A9	VCC[002]	VCC[069]
A10	VCC[003]	VCC[070]
A12	VCC[004]	VCC[071]
A13	VCC[005]	VCC[072]
A15	VCC[006]	VCC[073]
A17	VCC[007]	VCC[074]
A18	VCC[008]	VCC[075]
A20	VCC[009]	VCC[076]
B7	VCC[010]	VCC[077]
B8	VCC[011]	VCC[078]
B10	VCC[012]	VCC[079]
B12	VCC[013]	VCC[080]
B14	VCC[014]	VCC[081]
B15	VCC[015]	VCC[082]
B17	VCC[016]	VCC[083]
B18	VCC[017]	VCC[084]
B20	VCC[018]	VCC[085]
C8	VCC[019]	VCC[086]
C10	VCC[020]	VCC[087]
C12	VCC[021]	VCC[088]
C13	VCC[022]	VCC[089]
C15	VCC[023]	VCC[090]
C17	VCC[024]	VCC[091]
C18	VCC[025]	VCC[092]
D9	VCC[026]	VCC[093]
D10	VCC[027]	VCC[094]
D12	VCC[028]	VCC[095]
D14	VCC[029]	VCC[096]
D15	VCC[030]	VCC[097]
D17	VCC[031]	VCC[098]
D18	VCC[032]	VCC[099]
E7	VCC[033]	VCC[100]
E8	VCC[034]	
E10	VCC[035]	VCCP[01]
E12	VCC[036]	VCCP[02]
E13	VCC[037]	VCCP[03]
E15	VCC[038]	VCCP[04]
E17	VCC[039]	VCCP[05]
E20	VCC[040]	VCCP[06]
F9	VCC[041]	VCCP[07]
F7	VCC[042]	VCCP[08]
F9	VCC[043]	VCCP[09]
F10	VCC[044]	VCCP[10]
F12	VCC[045]	VCCP[11]
F14	VCC[046]	VCCP[12]
F15	VCC[047]	VCCP[13]
F17	VCC[048]	VCCP[14]
F18	VCC[049]	VCCP[15]
F20	VCC[050]	VCCP[16]
AA7	VCC[051]	VCCA[01]
AA9	VCC[052]	VCCA[02]
AA10	VCC[053]	VCCA[03]
AA12	VCC[054]	VCC[054]
AA13	VCC[055]	VCC[055]
AA15	VCC[056]	VCC[056]
AA17	VCC[057]	VCC[057]
AA18	VCC[058]	VCC[058]
AA20	VCC[059]	VCC[059]
AB9	VCC[060]	VCC[060]
AC10	VCC[061]	VCC[061]
AB10	VCC[062]	VCC[062]
AB12	VCC[063]	VCC[063]
AB14	VCC[064]	VCC[064]
AB15	VCC[065]	VCC[065]
AB17	VCC[066]	VCC[066]
AB18	VCC[067]	VCC[067]
	VCCA[01]	B26
	VCCA[02]	C26
	VCC[054]	AD6
	VCC[055]	AF5
	VCC[056]	AE5
	VCC[057]	VID2
	VCC[058]	VID3
	VCC[059]	VID4
	VCC[060]	VID5
	VCC[061]	VID6
	VCC[062]	VID6
	VCC[063]	VID6
	VCC[064]	VID6
	VCC[065]	VID6
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	VCC[100]	VID6



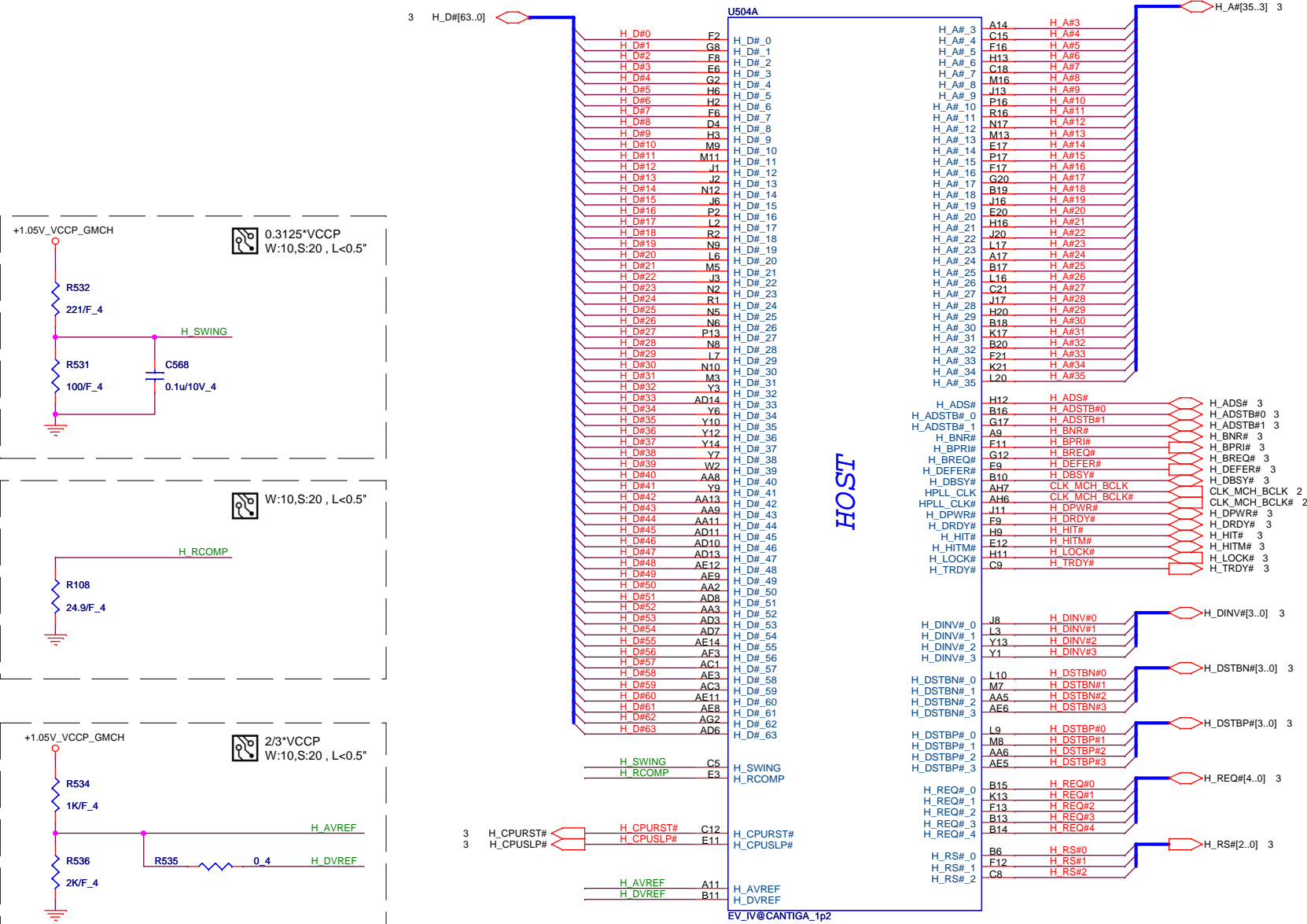
Layout Note: Route VCCSENSE and VSSSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of CPU.

Quanta Computer Inc.
PROJECT : TE1M

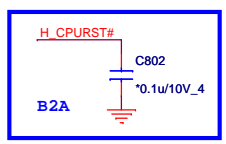
Size: Document Number CPU(2/2)- Power Rev: E3D
 Date: Monday, May 26, 2008 Sheet: 4 of 40


BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM



GM PN=> AJSLB940T05
PM PN=> AJSLB970T03





Quanta Computer Inc.
PROJECT : TE1M

Size	Document Number	Rev
	NB (1/7)- HOST	E3D
Date:	Monday, May 26, 2008	Sheet 5 of 40

BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM

GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

17 M_A_DQ[63:0]

U504D

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AM36	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AJ40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AJ44	SA_DQ_14
M A DQ15	AJ42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BA43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BB41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AV37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BB38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AV36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AJ11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AJ13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AJ10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AY8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AJ5	SA_DQ_52
M A DQ53	AJ6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M A BS#0	M_A_BS#0 16,17
SA_BS_1	BG18	M A BS#1	M_A_BS#1 16,17
SA_BS_2	AT25	M A BS#2	M_A_BS#2 16,17
SA_RAS#	BB20	M A RAS#	M_A_RAS# 16,17
SA_CAS#	BD20	M A CAS#	M_A_CAS# 16,17
SA_WE#	AY20	M A WE#	M_A_WE# 16,17
SA_DM_0	AM37	M A DM0	M_A_DM[7:0] 17
SA_DM_1	AT41	M A DM1	
SA_DM_2	AY41	M A DM2	
SA_DM_3	AJ39	M A DM3	
SA_DM_4	BB12	M A DM4	
SA_DM_5	AY6	M A DM5	
SA_DM_6	AT7	M A DM6	
SA_DM_7	AJ5	M A DM7	
SA_DQS_0	AJ44	M A DQS0	M_A_DQS[7:0] 17
SA_DQS_1	AT44	M A DQS1	
SA_DQS_2	BA43	M A DQS2	
SA_DQS_3	BC37	M A DQS3	
SA_DQS_4	AW12	M A DQS4	
SA_DQS_5	BC8	M A DQS5	
SA_DQS_6	AJ8	M A DQS6	
SA_DQS_7	AM7	M A DQS7	M_A_DQS#[7:0] 17
SA_DQS#_0	AJ43	M A DQS#0	
SA_DQS#_1	AT43	M A DQS#1	
SA_DQS#_2	BA44	M A DQS#2	
SA_DQS#_3	BD37	M A DQS#3	
SA_DQS#_4	AY12	M A DQS#4	
SA_DQS#_5	BD8	M A DQS#5	
SA_DQS#_6	AJ9	M A DQS#6	
SA_DQS#_7	AM8	M A DQS#7	
SA_MA_0	BA21	M A A0	M_A_A[14:0] 16,17
SA_MA_1	BC24	M A A1	
SA_MA_2	BG24	M A A2	
SA_MA_3	BH24	M A A3	
SA_MA_4	BG25	M A A4	
SA_MA_5	BA24	M A A5	
SA_MA_6	BD24	M A A6	
SA_MA_7	BG27	M A A7	
SA_MA_8	BF25	M A A8	
SA_MA_9	AW24	M A A9	
SA_MA_10	BC21	M A A10	
SA_MA_11	BG26	M A A11	
SA_MA_12	BH26	M A A12	
SA_MA_13	BH17	M A A13	
SA_MA_14	AY25	M A A14	

EV_IV@CANTIGA_1p2

17 M_B_DQ[63:0]

U504E

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AJ47	SB_DQ_8
M B DQ9	AJ46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BC38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG32	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BE11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AJ3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M B BS#0	M_B_BS#0 16,17
SB_BS_1	BB17	M B BS#1	M_B_BS#1 16,17
SB_BS_2	BB33	M B BS#2	M_B_BS#2 16,17
SB_RAS#	AJ17	M B RAS#	M_B_RAS# 16,17
SB_CAS#	BG16	M B CAS#	M_B_CAS# 16,17
SB_WE#	BF14	M B WE#	M_B_WE# 16,17
SB_DM_0	AM47	M B DM0	M_B_DM[7:0] 17
SB_DM_1	BD40	M B DM1	
SB_DM_2	BF35	M B DM2	
SB_DM_3	BF35	M B DM3	
SB_DM_4	BG11	M B DM4	
SB_DM_5	BA3	M B DM5	
SB_DM_6	AP1	M B DM6	
SB_DM_7	AK2	M B DM7	
SB_DQS_0	AL47	M B DQS0	M_B_DQS[7:0] 17
SB_DQS_1	AV48	M B DQS1	
SB_DQS_2	BG41	M B DQS2	
SB_DQS_3	BC37	M B DQS3	
SB_DQS_4	BH9	M B DQS4	
SB_DQS_5	BB2	M B DQS5	
SB_DQS_6	AJ1	M B DQS6	
SB_DQS_7	AN6	M B DQS7	
SB_DQS#_0	AL46	M B DQS#0	M_B_DQS#[7:0] 17
SB_DQS#_1	AV47	M B DQS#1	
SB_DQS#_2	BH41	M B DQS#2	
SB_DQS#_3	BH37	M B DQS#3	
SB_DQS#_4	BG9	M B DQS#4	
SB_DQS#_5	BC2	M B DQS#5	
SB_DQS#_6	AT2	M B DQS#6	
SB_DQS#_7	AN5	M B DQS#7	
SB_MA_0	AV17	M B A0	M_B_A[14:0] 16,17
SB_MA_1	BA25	M B A1	
SB_MA_2	BC25	M B A2	
SB_MA_3	AJ25	M B A3	
SB_MA_4	AW25	M B A4	
SB_MA_5	BB28	M B A5	
SB_MA_6	AJ28	M B A6	
SB_MA_7	AV23	M B A7	
SB_MA_8	AT33	M B A8	
SB_MA_9	BD33	M B A9	
SB_MA_10	BB16	M B A10	
SB_MA_11	AV33	M B A11	
SB_MA_12	AV33	M B A12	
SB_MA_13	BH15	M B A13	
SB_MA_14	AJ33	M B A14	

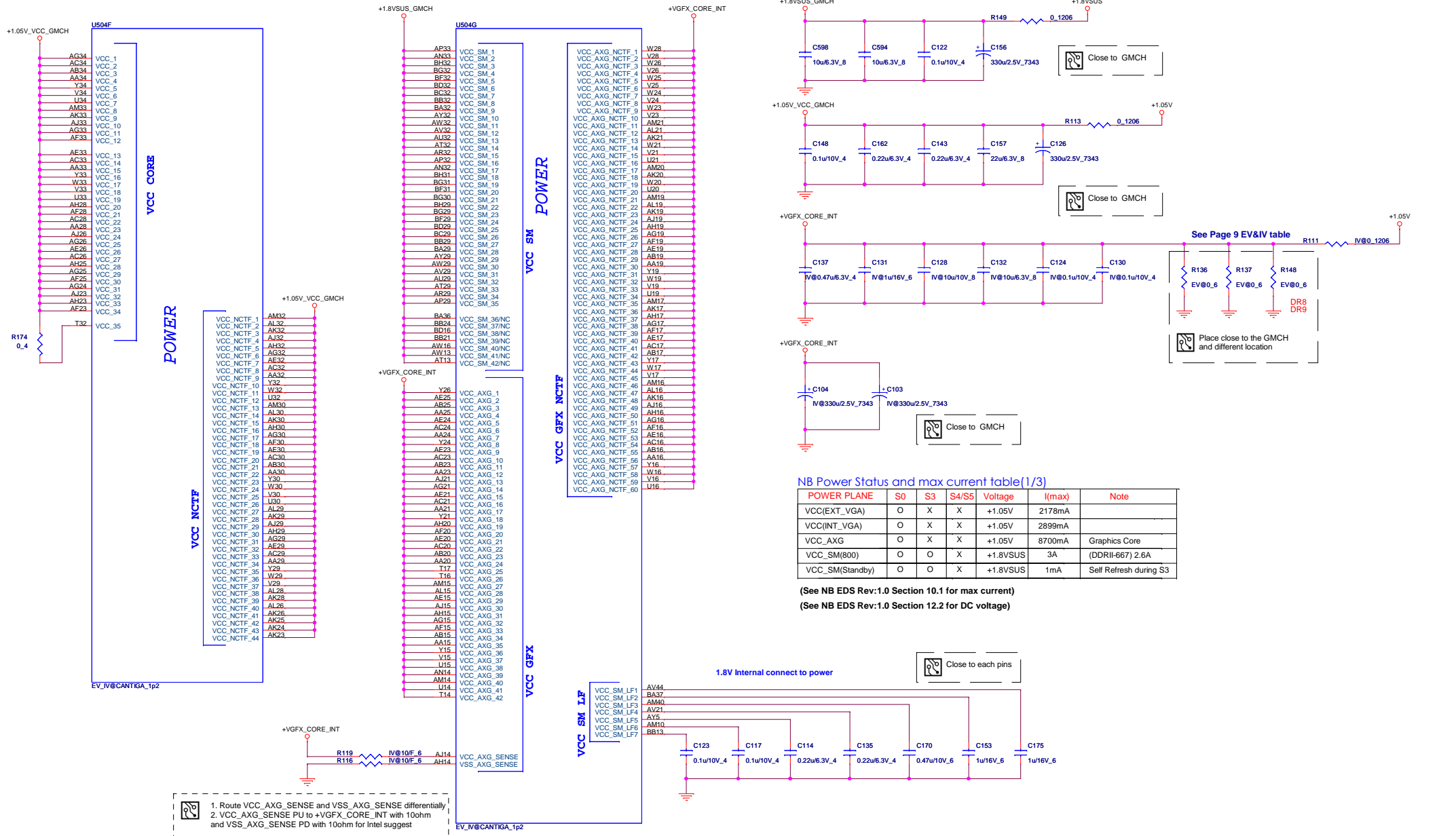
EV_IV@CANTIGA_1p2



Size	Document Number	Rev
	NE (3/7)- DDRII	E3D
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GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

BOM Option Table	
Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM



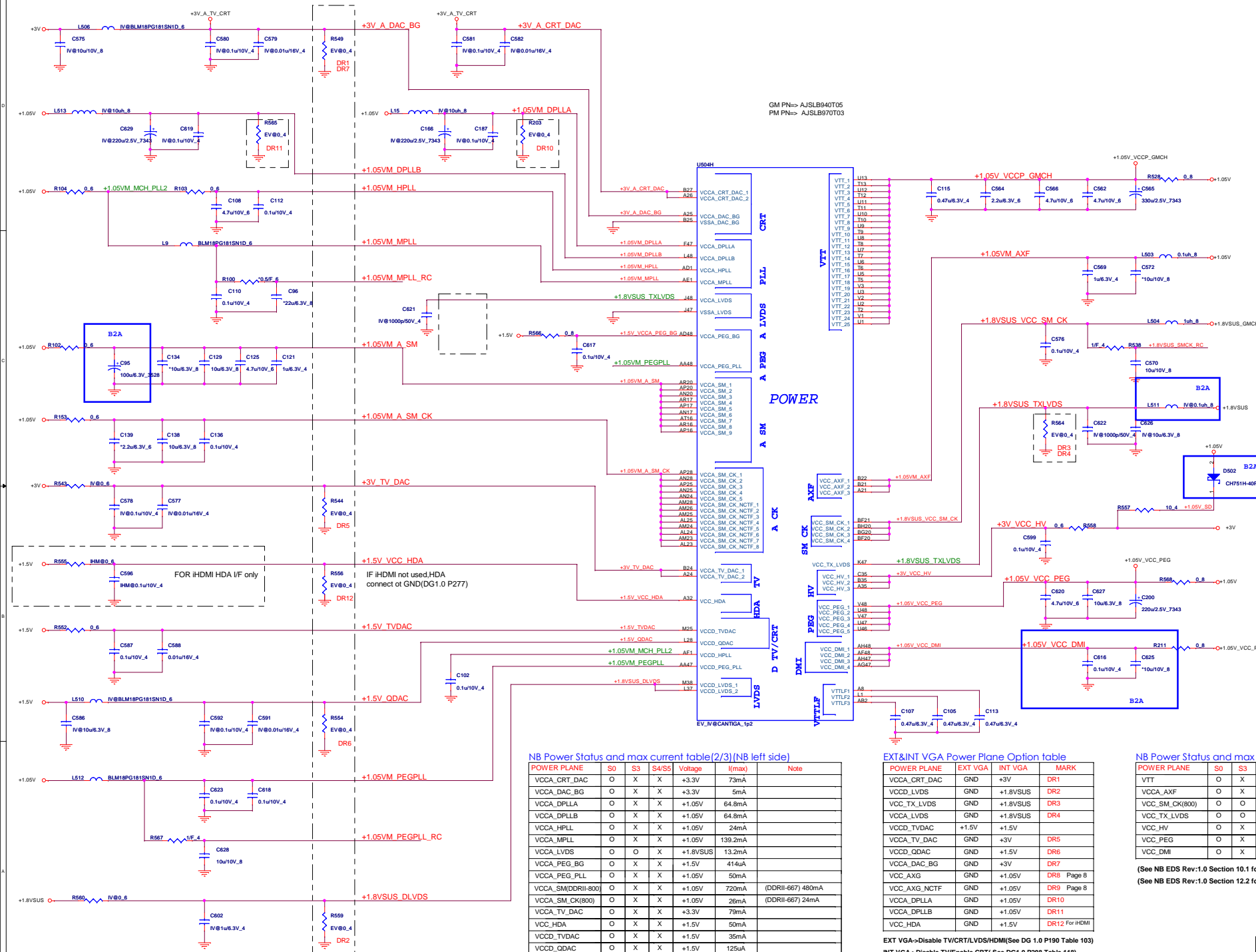
NB Power Status and max current table(1/3)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AGX	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

1. Route VCC_AGX_SENSE and VSS_AGX_SENSE differentially
2. VCC_AGX_SENSE PU to +VGFX_CORE_INT with 10ohm and VSS_AGX_SENSE PD with 10ohm for intel suggest

Reference	Description
IV@	INT VGA
EV@	EXT VGA
IHM@	INT HDMI
EV_IV@	EV&IV diff. BOM



GM PN=> AJSLB940T05
PM PN=> AJSLB970T03

NB Power Status and max current table(2/3)(NB left side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCCA_CRT_DAC	0	X	X	+3.3V	73mA	
VCCA_DAC_BG	0	X	X	+3.3V	5mA	
VCCA_DPLLA	0	X	X	+1.05V	64.8mA	
VCCA_DPLLB	0	X	X	+1.05V	64.8mA	
VCCA_HPPLL	0	X	X	+1.05V	24mA	
VCCA_MPLL	0	X	X	+1.05V	139.2mA	
VCCA_LVDS	0	0	X	+1.8VSUS	13.2mA	
VCCA_PEG_BG	0	X	X	+1.5V	414uA	
VCCA_PEG_PLL	0	X	X	+1.05V	50mA	
VCCA_SM(DDR1800)	0	X	X	+1.05V	720mA	(DDR11-667) 480mA
VCCA_SM_CK(800)	0	X	X	+1.05V	26mA	(DDR11-667) 24mA
VCCA_TV_DAC	0	X	X	+3.3V	79mA	
VCC_HDA	0	X	X	+1.5V	50mA	
VCCD_TV_DAC	0	X	X	+1.5V	35mA	
VCCD_QDAC	0	X	X	+1.5V	125uA	
VCCD_HPPLL	0	X	X	+1.05V	157mA	
VCCD_MPLL	0	X	X	+1.05V	157mA	
VCCD_PEG_PLL	0	X	X	+1.05V	50mA	
VCCD_LVDS	0	0	X	+1.8VSUS	60mA	

EXT&INT VGA Power Plane Option table

POWER PLANE	EXT VGA	INT VGA	MARK
VCCA_CRT_DAC	GND	+3V	DR1
VCCD_LVDS	GND	+1.8VSUS	DR2
VCC_TX_LVDS	GND	+1.8VSUS	DR3
VCCA_LVDS	GND	+1.8VSUS	DR4
VCCD_TV_DAC	GND	+3V	DR5
VCCD_QDAC	GND	+1.5V	DR6
VCCA_DAC_BG	GND	+3V	DR7
VCCA_AXG	GND	+1.05V	DR8 Page 8
VCC_AXG_NCTF	GND	+1.05V	DR9 Page 8
VCCA_DPLLA	GND	+1.05V	DR10
VCCA_DPLLB	GND	+1.05V	DR11
VCC_HDA	GND	+1.5V	DR12 For IHDMI

EXT VGA->Disable TV/CRT/LVDS/HDMI(See DG 1.0 P190 Table 103)
INT VGA->Disable TV/Enable CRT (See DG1.0 P208 Table 118)
INT VGA->Disable HDMI(See DG 1.0 P277 section 3.10.4)

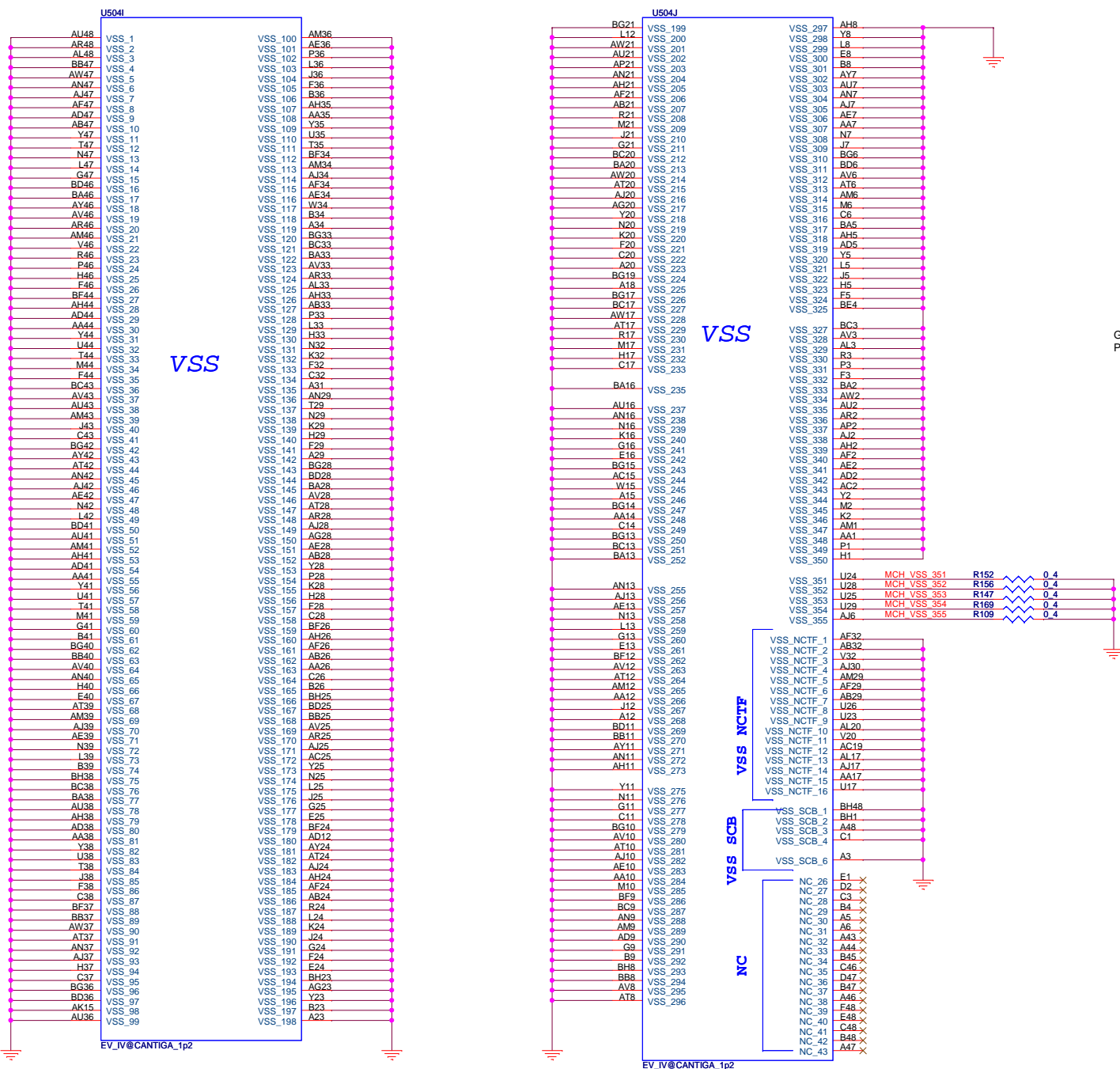
NB Power Status and max current table(3/3)(NB Right side)

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VTT	0	X	X	+1.05V	852mA	FSB at 1067MHz
VCCA_AXF	0	X	X	+1.05V	322mA	
VCC_SM_CK(800)	0	0	X	+1.8VSUS	124mA	(DDR11-667) 120mA
VCC_TX_LVDS	0	0	X	+1.8VSUS	119mA	
VCC_HV	0	X	X	+1.05V	106mA	
VCC_PEG	0	X	X	+1.05V	1782mA	
VCC_DMI	0	X	X	+1.05V	456mA	


(See NB EDS Rev:1.0 Section 10.1 for max current)
(See NB EDS Rev:1.0 Section 12.2 for DC voltage)

BOM Option Table

Reference	Description
EV_IV@	EV&IV diff. BOM



GM PN=> AJSLB940T05
PM PN=> AJSLB970T03



Quanta Computer Inc.
PROJECT : TE1M

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	NB (67)- VSS	E3D
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BOM Option Table

Reference	Description
iTPM@	Internal TPM


North Bridge Strap Pin Configuration Table

(See DG 1.0 P295 Table 184)
(See NB EDS 1.0 P187 Table 74)

Pin Name	Strap description	Configuration	PU<4.02K> PD <2.21K>	Note
CFG[2:0]	FSB Frequency Select	[000]= FSB 1066MHz [010] = FSB 800MHz [011] = FSB 667MHz	See Page 2 FSB selection table	
CFG[4:3]	Reserved			
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)	6 MCH_CFG_5	
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)	6 MCH_CFG_6	
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)	6 MCH_CFG_7	
CFG8	Reserved			
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)	6 MCH_CFG_9	
CFG10	PCIE Loopback enable	0 = Enabled 1 = Disabled (Default)	6 MCH_CFG_10	
CFG11	Reserved			
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)	6 MCH_CFG_12	
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)	6 MCH_CFG_13	
CFG[15:14]	Reserved			
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)	6 MCH_CFG_16	
CFG[18:17]	Reserved			
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed	6 MCH_CFG_19	
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIE	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIE is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIE are operating simultaneously via PEG port	6 MCH_CFG_20	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI/DP Device Present(Default) 1 = SDVO/HDMI/DP Device present	6,21 SDVO_CTRLDATA	Reference PAGE21 R185
L_DDC_DATA	Local Flat Panel(LFP) Present	0 = LFP Disable(Default) 1 = LFP Card Present,PCIE disable	6,19 INT_LVDS_EDIDDATA	
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present	6 DDPC_CTRLDATA	

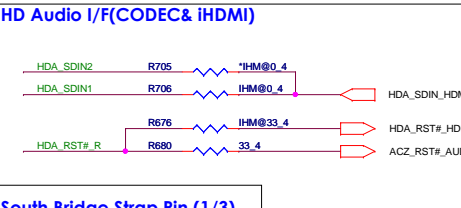
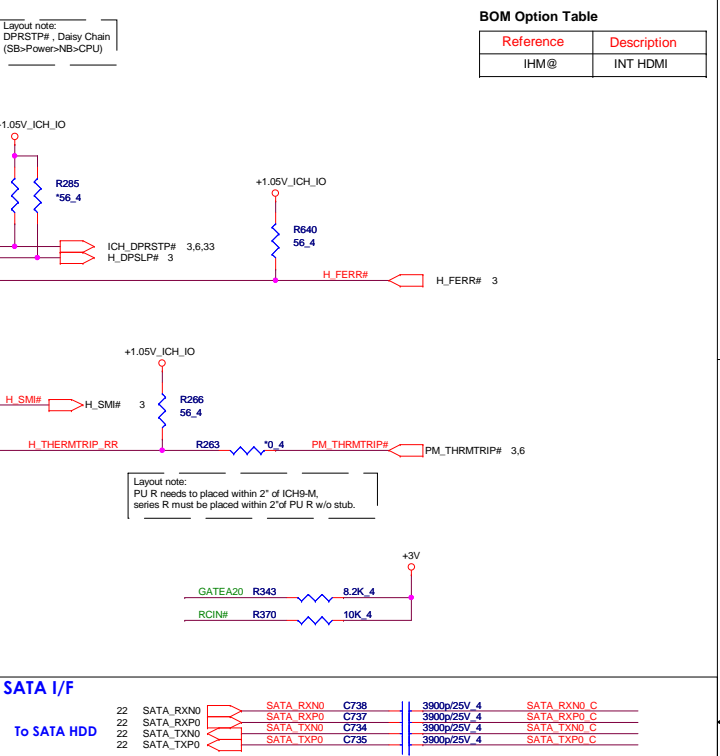
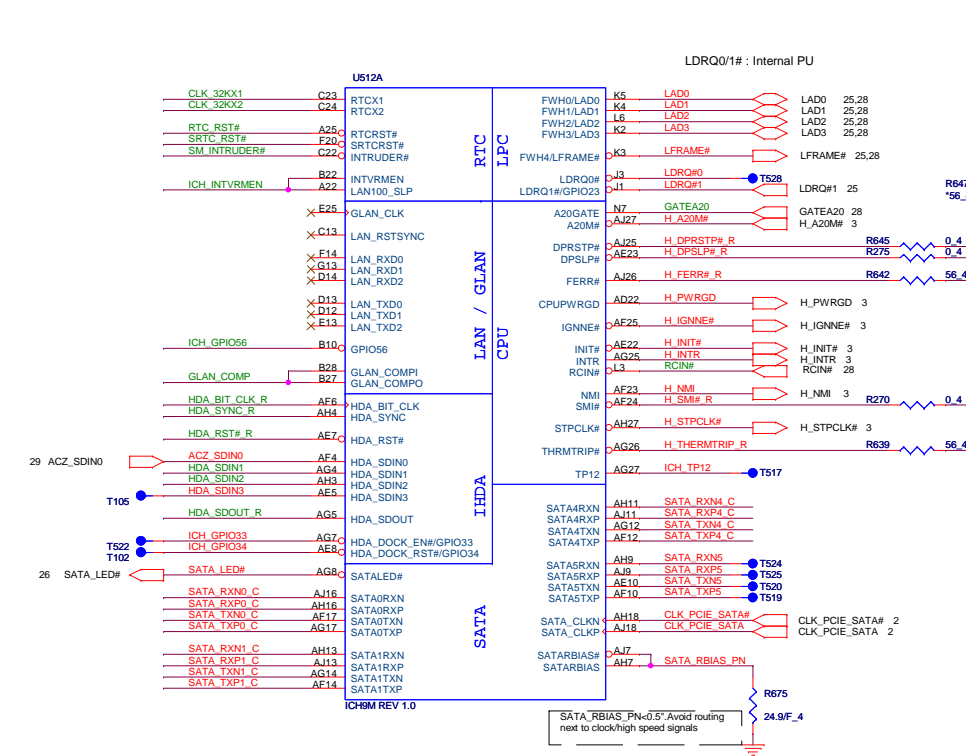
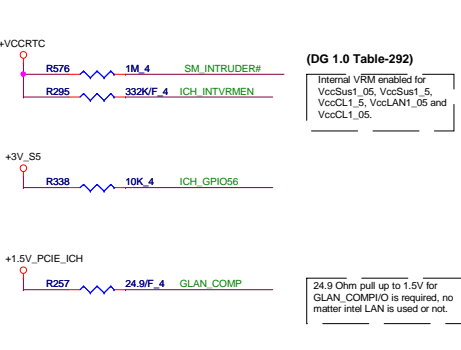
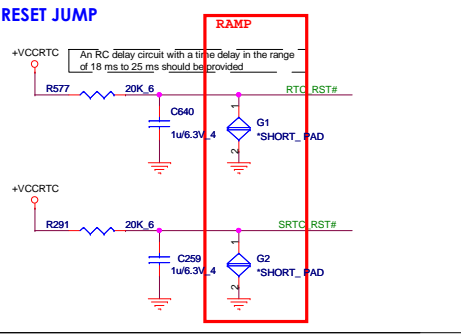
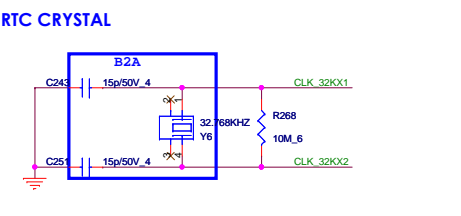
Enable iTPM Table

PAGE	Net Name	PU & PD	NOTE
11	MCH_CFG_6	PD 10K to GND	NB Strap pin
13	SPL_MOSI	PU 20K to +3V_S5	SB Strap pin
14	CLGPIO5	PU 10K to +3V_S5	SB Strap pin



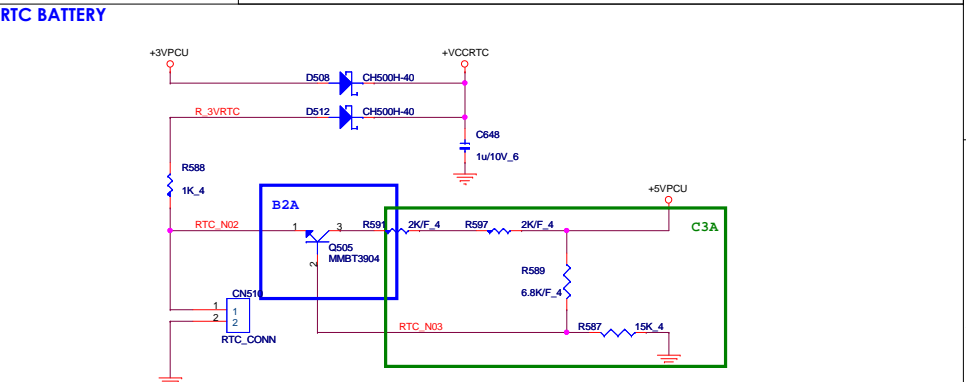
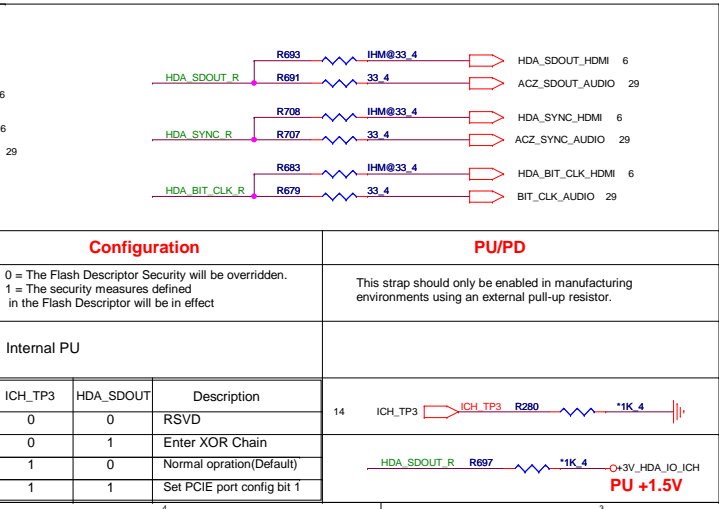
Quanta Computer Inc.
PROJECT : TE1M

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	NB (77)- STRAP PIN	E3D
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South Bridge Strap Pin (1/3)

Pin Name	Strap description	Sampled	Configuration	PUP/PD													
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect	This strap should only be enabled in manufacturing environments using an external pull-up resistor.													
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU														
TP3	XOR Chain Entrance	PWROK	<table border="1"> <thead> <tr> <th>ICH_TP3</th> <th>HDA_SDOUR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>RSVD</td> </tr> <tr> <td>0</td> <td>1</td> <td>Enter XOR Chain</td> </tr> </tbody> </table>	ICH_TP3	HDA_SDOUR	Description	0	0	RSVD	0	1	Enter XOR Chain	<table border="1"> <tbody> <tr> <td>ICH_TP3</td> <td>ICH_TP3</td> <td>R280</td> <td>*1K_4</td> </tr> </tbody> </table>	ICH_TP3	ICH_TP3	R280	*1K_4
ICH_TP3	HDA_SDOUR	Description															
0	0	RSVD															
0	1	Enter XOR Chain															
ICH_TP3	ICH_TP3	R280	*1K_4														
HDA_SDOUR	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	<table border="1"> <thead> <tr> <th>ICH_TP3</th> <th>HDA_SDOUR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>0</td> <td>Normal operation(Default)</td> </tr> <tr> <td>1</td> <td>1</td> <td>Set PCIe port config bit 1</td> </tr> </tbody> </table>	ICH_TP3	HDA_SDOUR	Description	1	0	Normal operation(Default)	1	1	Set PCIe port config bit 1	<table border="1"> <tbody> <tr> <td>HDA_SDOUR</td> <td>R697</td> <td>*1K_4</td> <td>+3V_HDA_IO_ICH</td> </tr> </tbody> </table>	HDA_SDOUR	R697	*1K_4	+3V_HDA_IO_ICH
ICH_TP3	HDA_SDOUR	Description															
1	0	Normal operation(Default)															
1	1	Set PCIe port config bit 1															
HDA_SDOUR	R697	*1K_4	+3V_HDA_IO_ICH														



Quanta Computer Inc.
PROJECT : TE1M

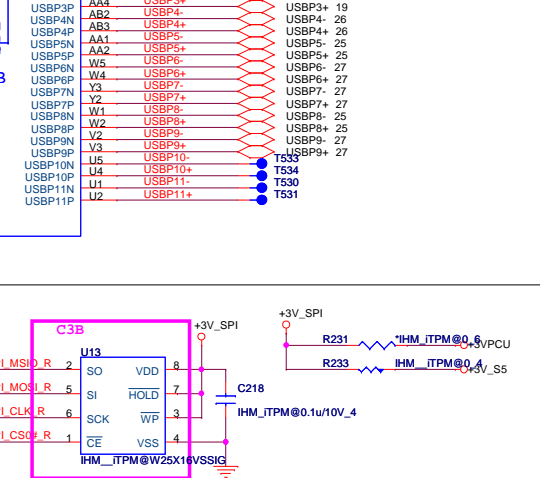
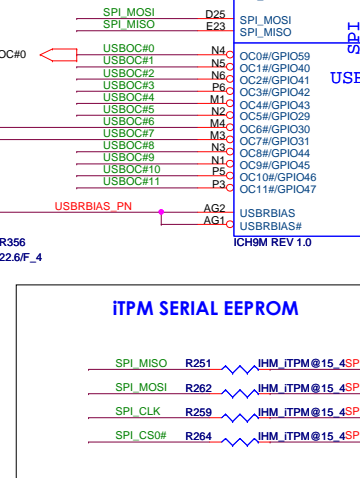
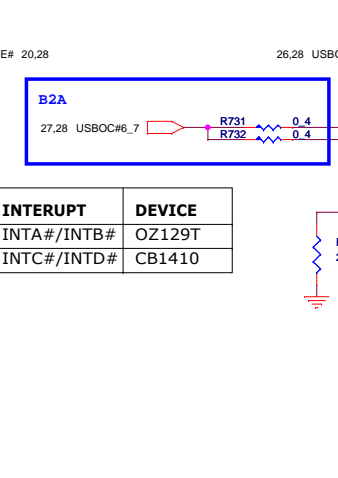
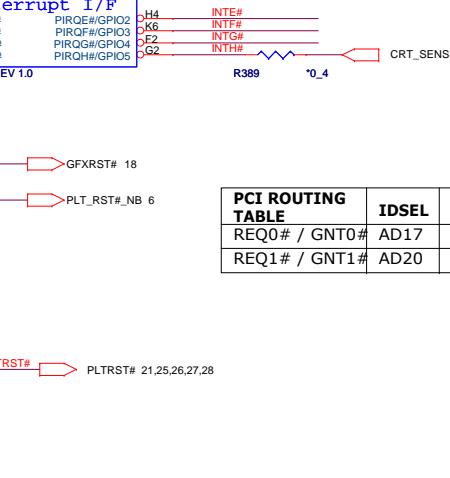
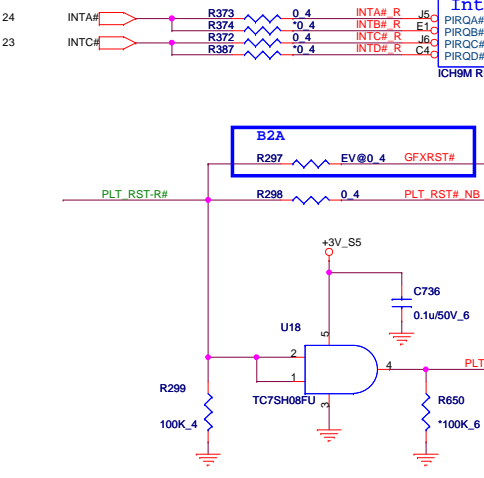
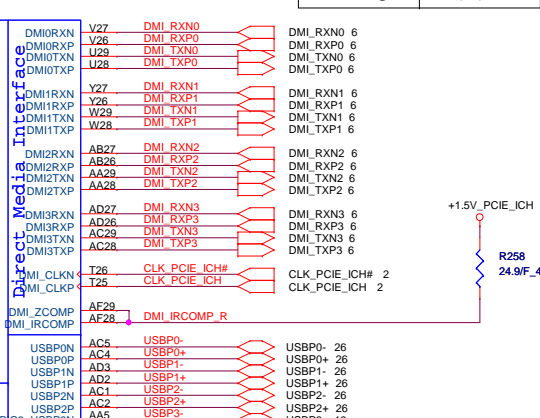
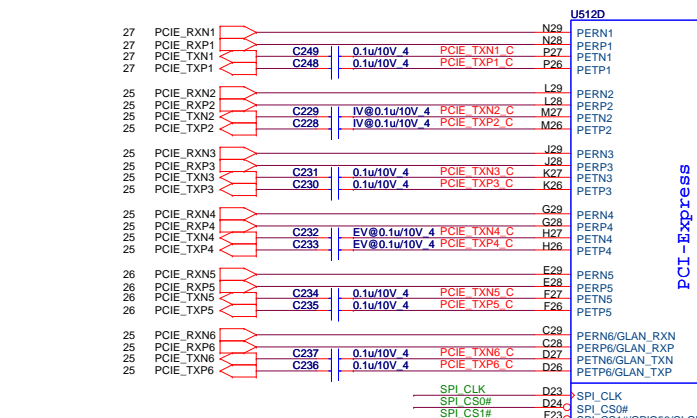
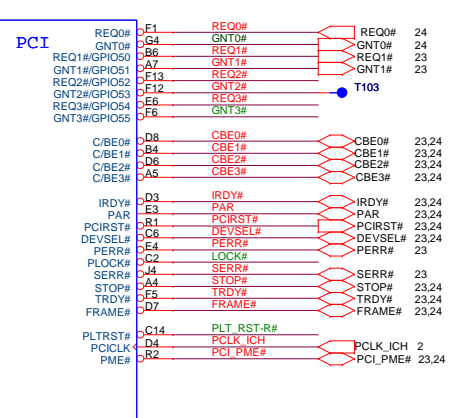
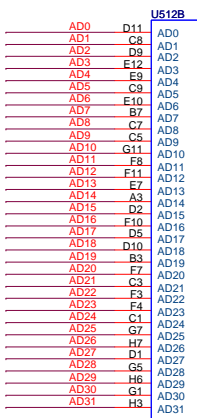
Size: Document Number: SB (1/4)- HOST Rev: E3D
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PCI/PCI-E/USB/DMI/SPI

BOM Option Table

Reference	Description
IV@	INT VGA
EV@	EXT VGA
ITPM@	Internal TPM

23,24 AD[0..31]

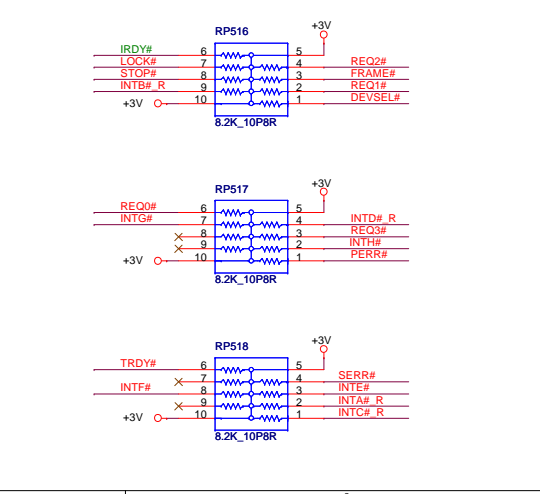


PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD17	INTA#/INTB#	OZ129T
REQ1# / GNT1#	AD20	INTC#/INTD#	CB1410

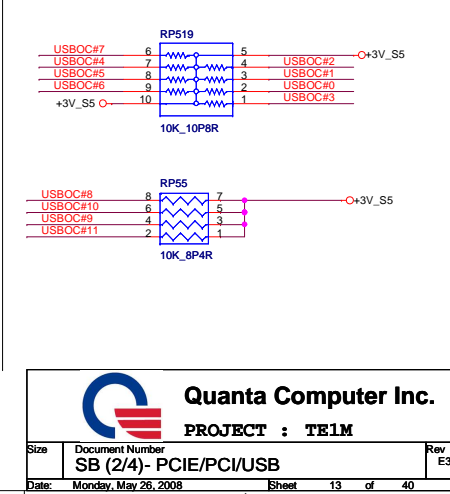
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD	
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0		
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default		
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default		
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default	GNT3# R376 *1K 4	
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable	SPI_MOSI R607 *TPM@20K 4 +3V_S5	
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT0#	Boot Location	GNT0# R375 *1K 4
			SPI_CS#1	SPI(Default)	
SPI_CS#1 / INTCS#1	Boot BIOS Selection 1	CLPWROK	0	PCI	
			1	LPC	SPI_CS#1 R267 *1K 4

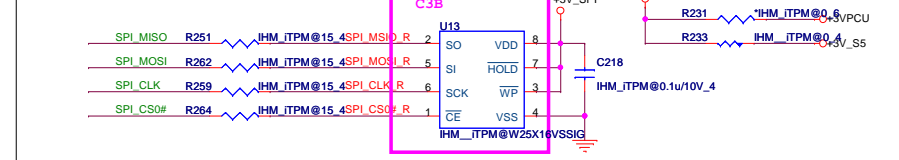
PCI PULL-UP



USBOC# PULL-UP



ITPM SERIAL EEPROM

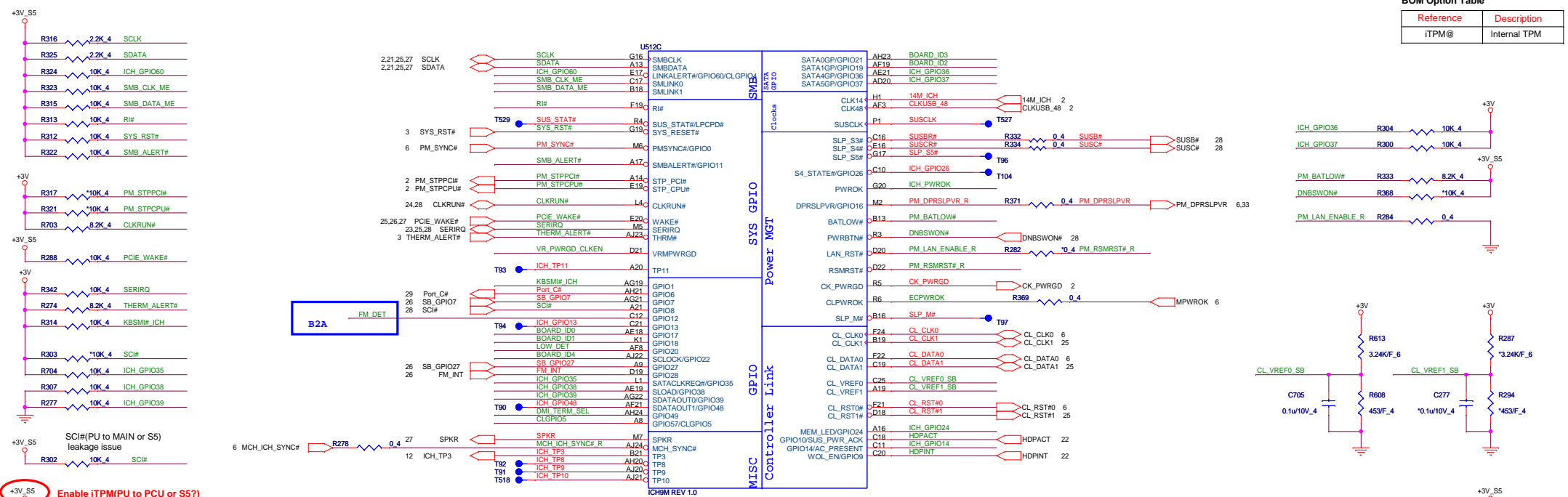


hsemail@protonmail.com
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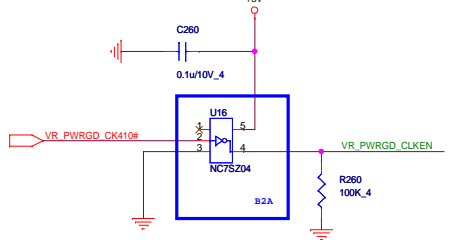
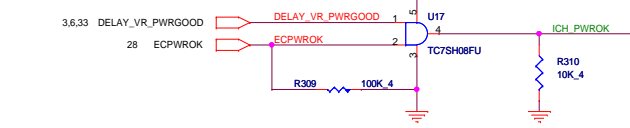
Size Document Number
SB (2/4)- PCIE/PCI/USB
Date: Monday, May 26, 2008 Sheet 13 of 40 Rev E3D

BOM Option Table	
Reference	Description
ITPM@	Internal TPM

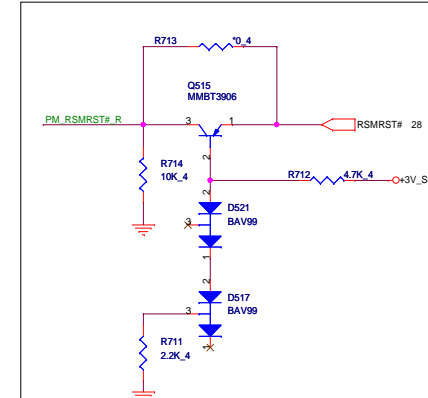
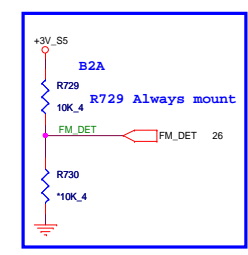


B2A FM_DET

DELAY_VR_PWRGOOD need PU 2K To +3V.
ZS2 PU at power side(NEEDED CHECK PWR CKT)

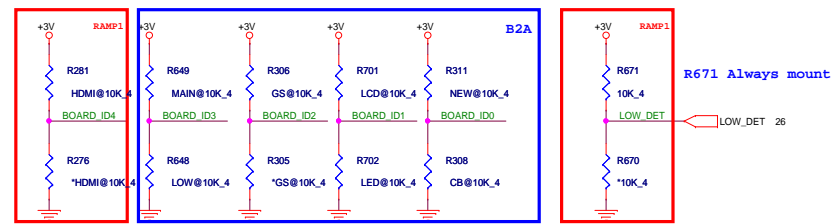


Board ID	ID4	ID3	ID2	ID1	ID0	M/L	FM
NEW CARD					H	L	
CARD BUS					L		
CCFL Panel				H			
LED Panel				L			
W/ G-SENSOR			H				
W/O G-SENSOR			L				
Main stream ID		H					
Low Cost ID		L					
W/ HDMI	H						
W/O HDMI	L						
W/O Low Cost board					H	L	
W Low Cost					L		
W/O FM							H
W FM							L



South Bridge Strap Pin (3/3)

Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	SPKR R341 1K_4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R269 1K_4

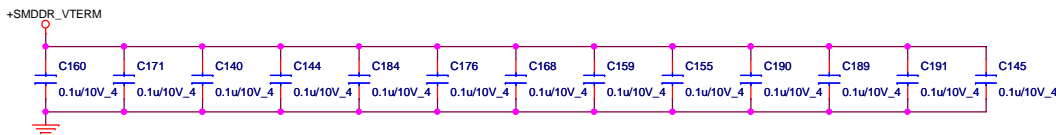


DDR2 Dual channel A/B PULL UP

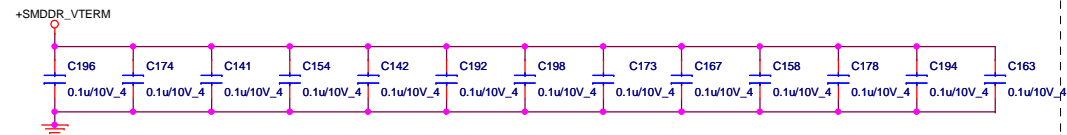
BOM Option Table

Reference	Description
N/A	N/A

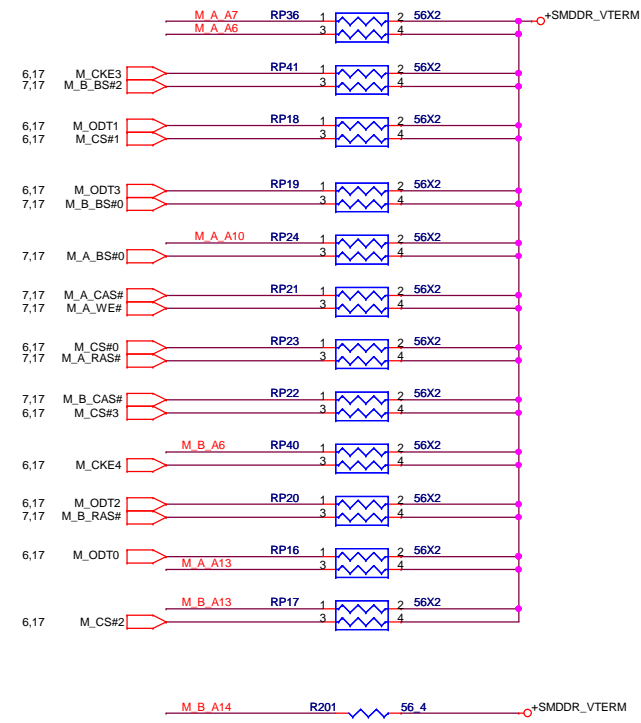
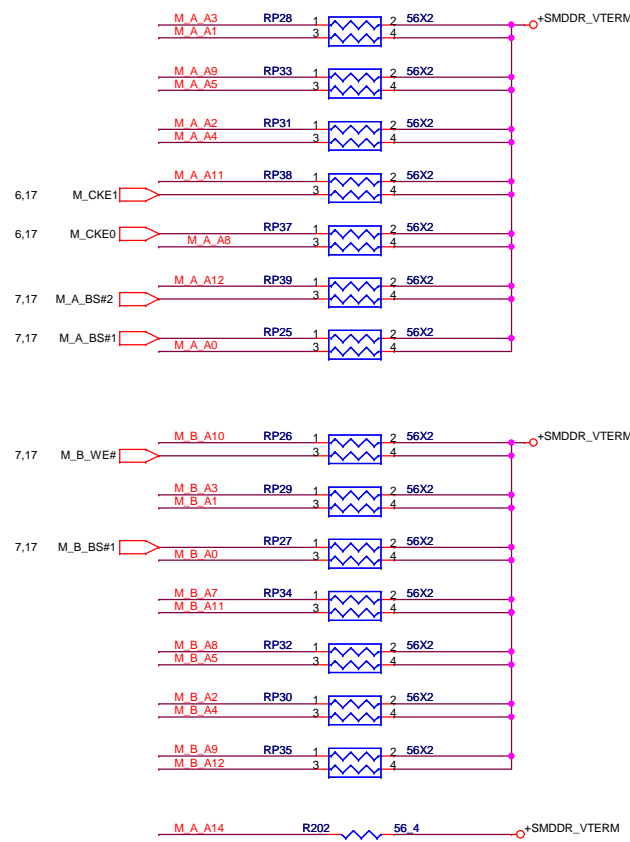
DDRII A CHANNEL




DDRII B CHANNEL



Place one cap close to every 2 pull-up resistor terminated to SMDDR_VTERM

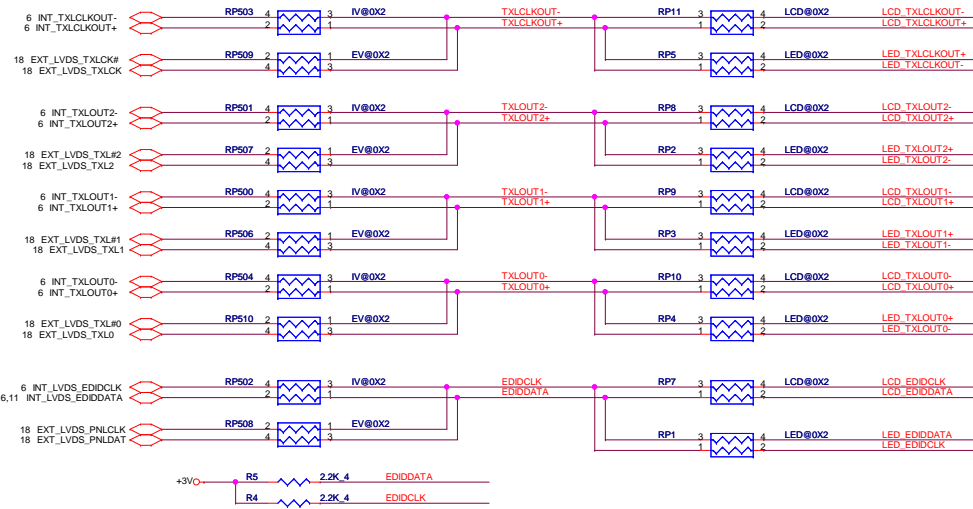




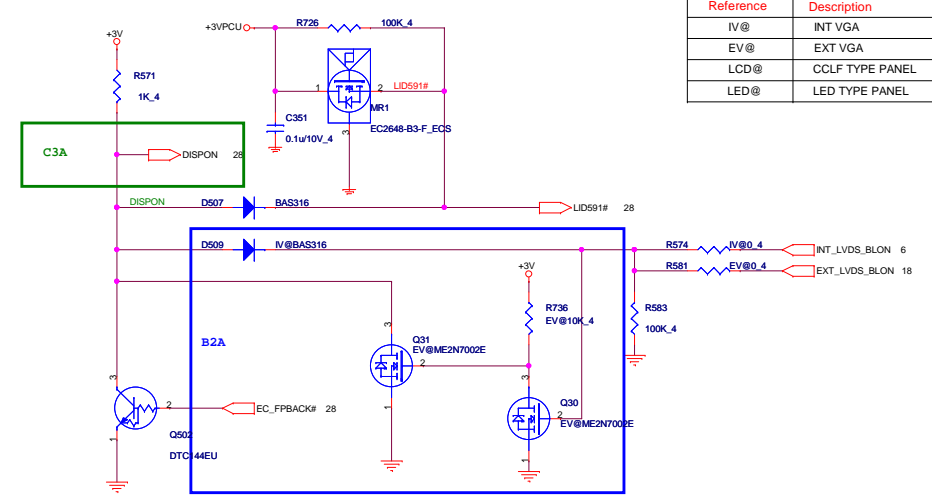
Quanta Computer Inc.
PROJECT : TELM

Size	Document Number	Rev
DDR RES. ARRAY		E3D
Date: Monday, May 26, 2008	Sheet	16 of 40

LVDS SIGNALS

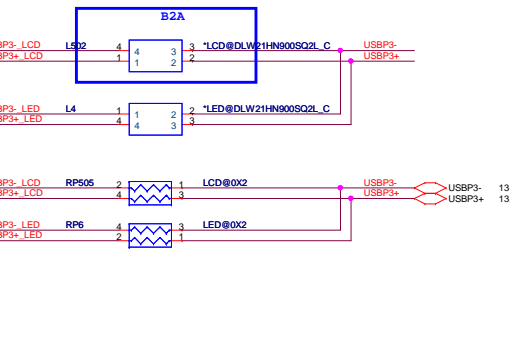
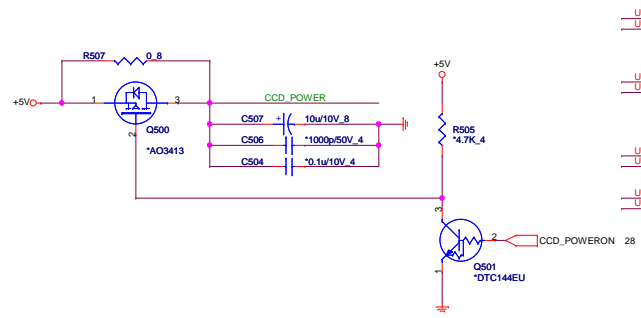


HALL SENSOR & BACK LIGHT SWITCH

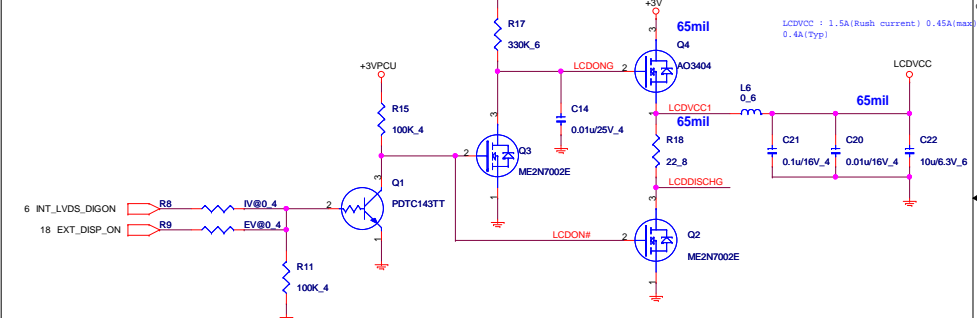


BOM Option Table	
Reference	Description
IV@	INT VGA
EV@	EXT VGA
LCD@	CCLF TYPE PANEL
LED@	LED TYPE PANEL

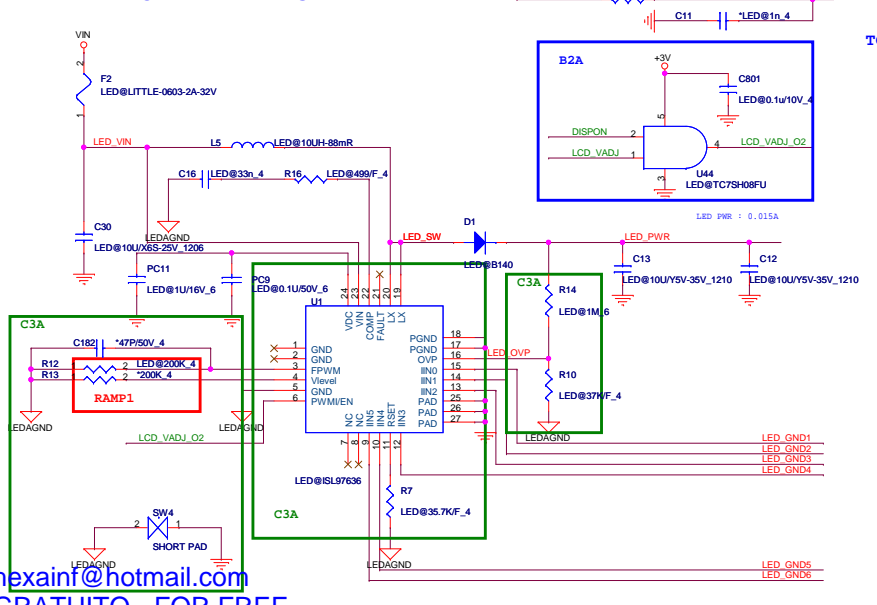
CCD POWER SWITCH



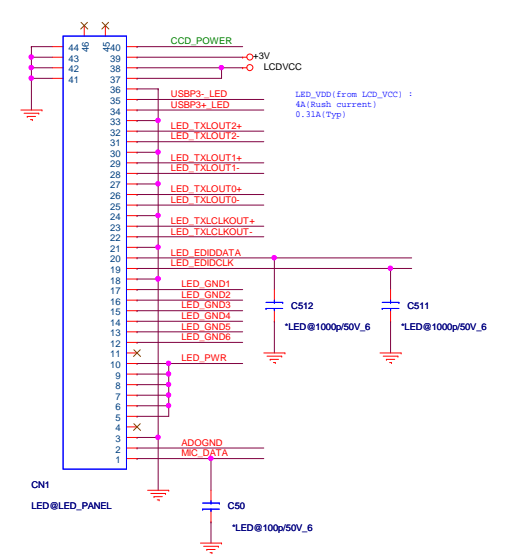
LCD POWER SWITCH



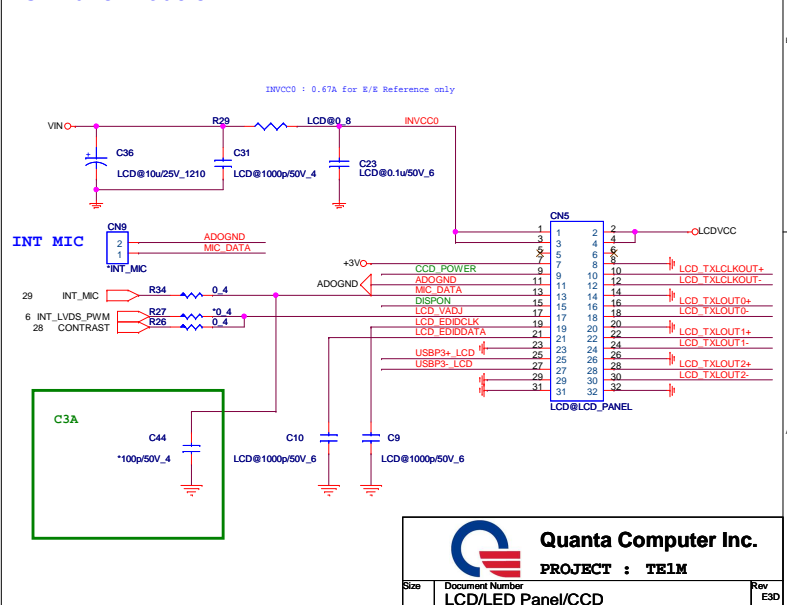
LED PANEL POWER DRIVER IC



TOSHIBA LED Panel Module



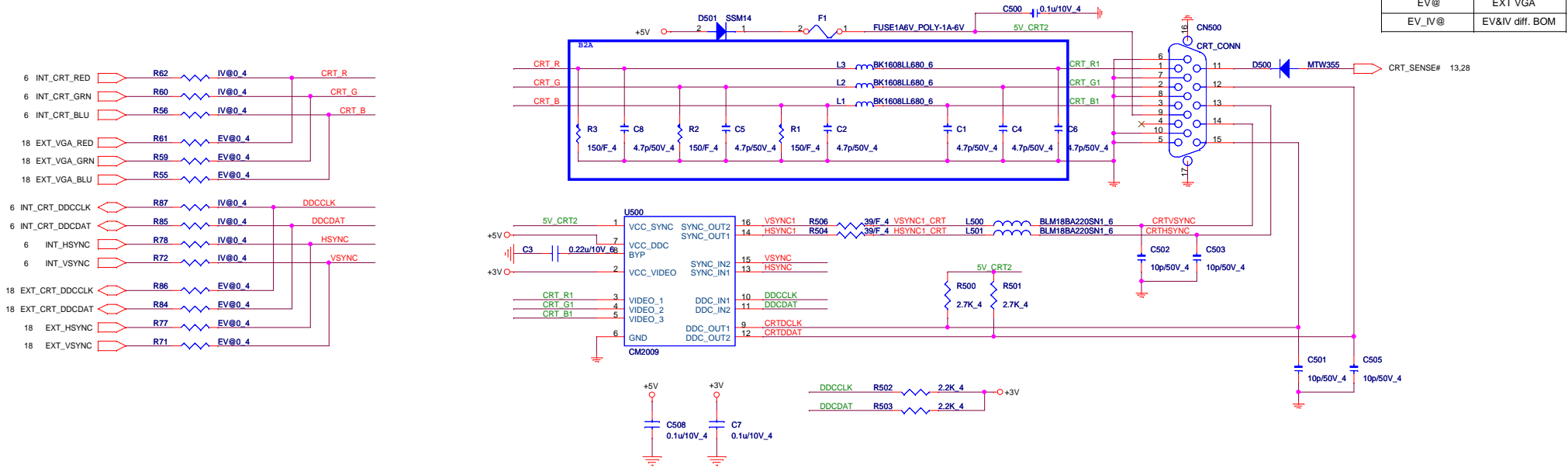
LCD Panel Module



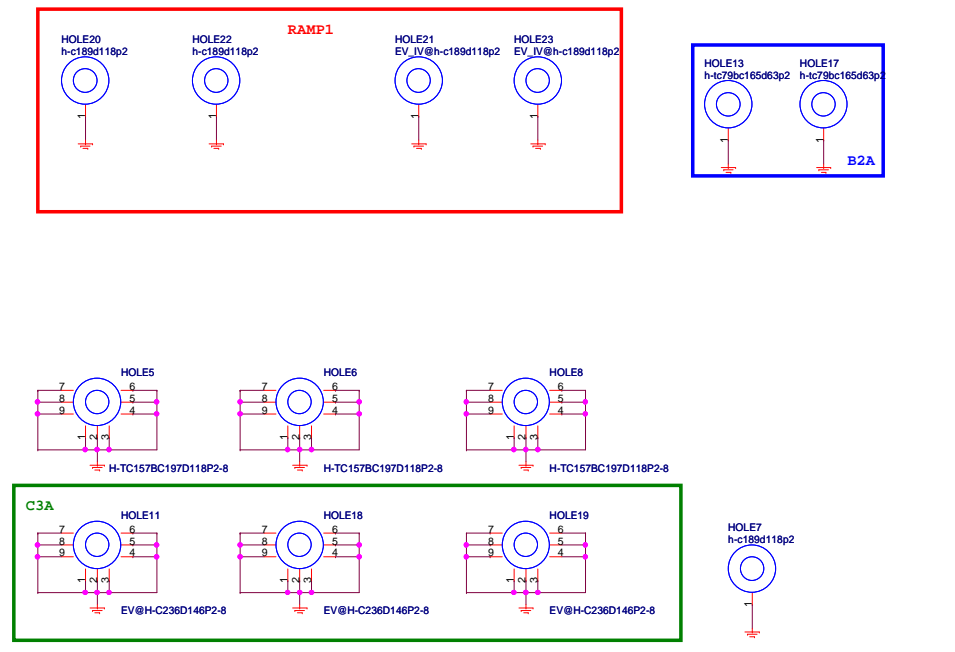
hexaint@hotmail.com
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CRT CONN & DDC LEVEL SHIFT IC

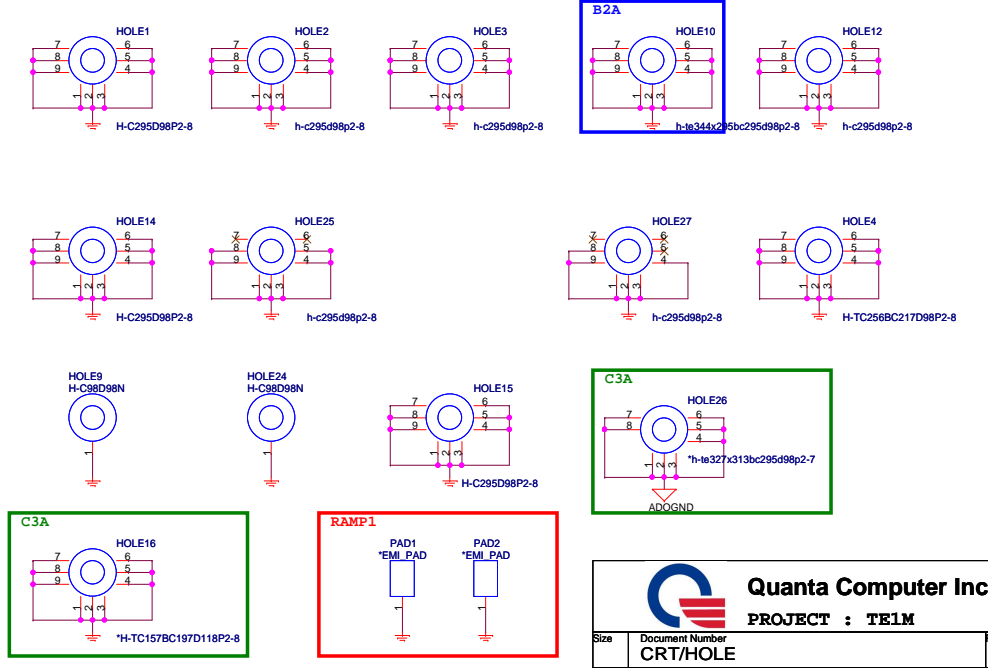
Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM



HOLE & NUTS



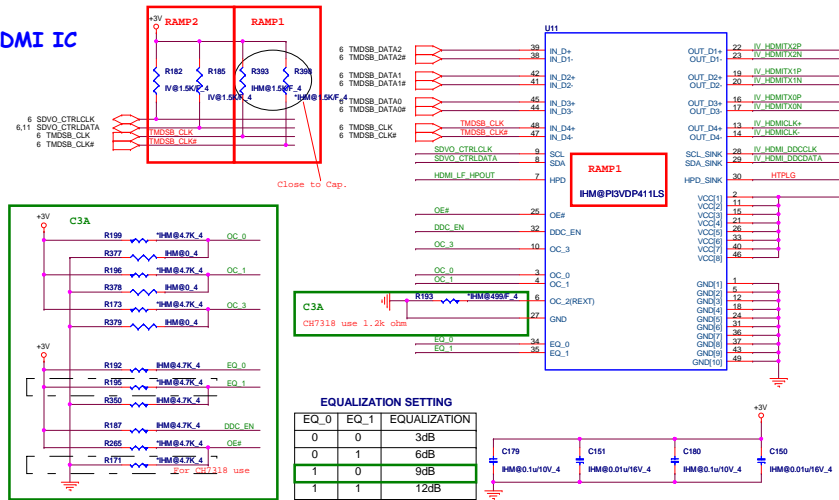
NUTS NEED RATING TOP or BOT (NUT don't use *)



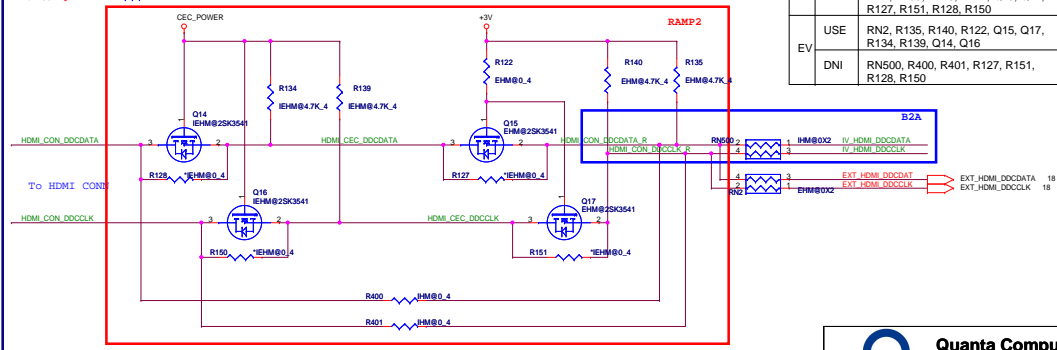
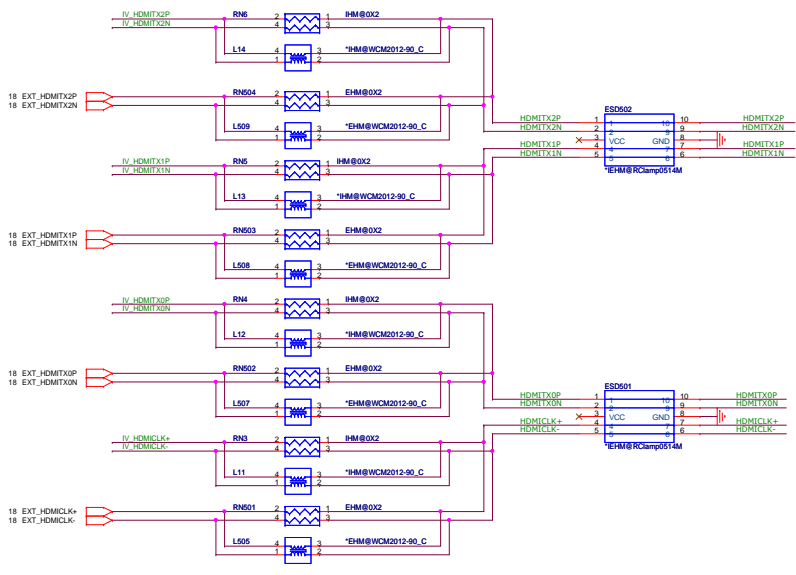
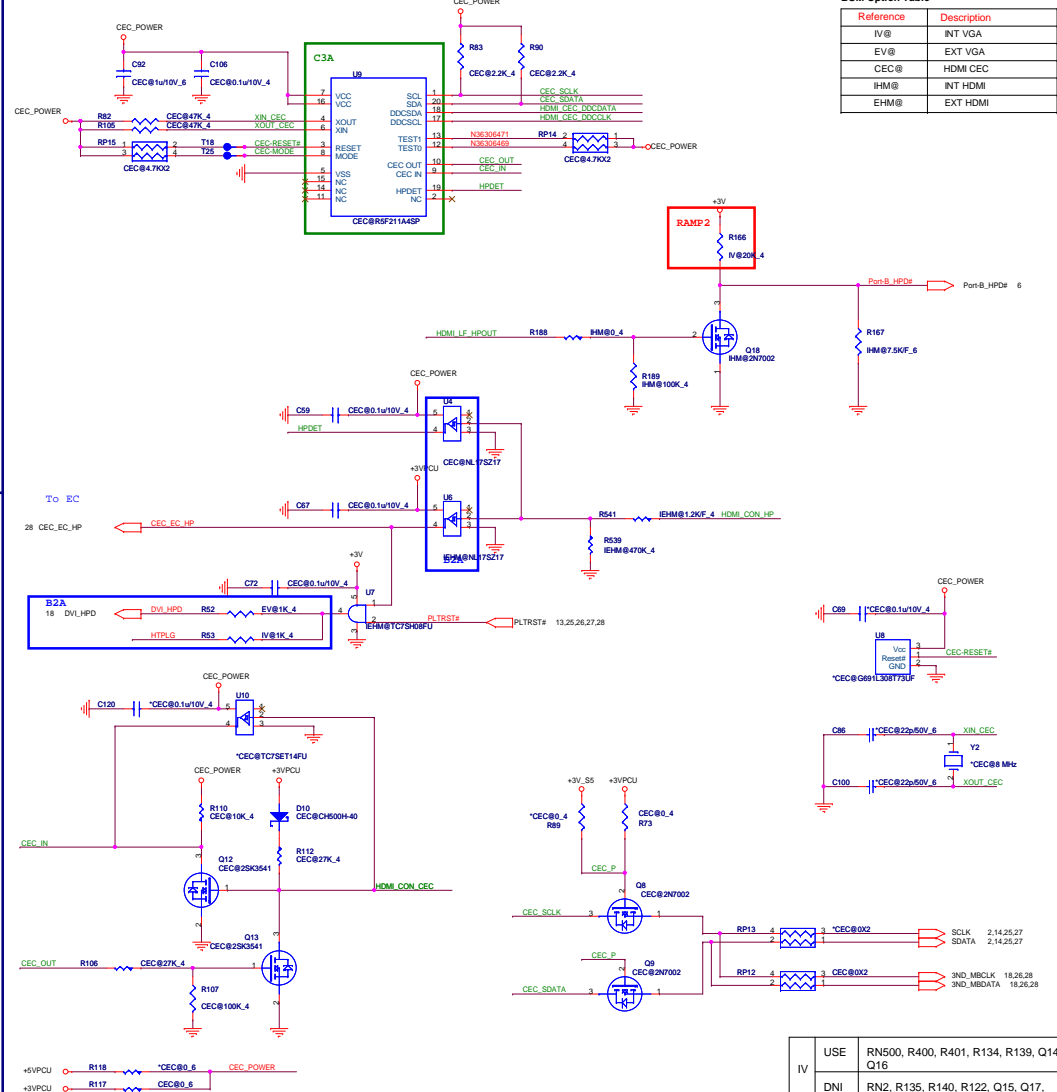
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Size	Document Number	Rev
	CRT/HOLE	E3D
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HDMI IC

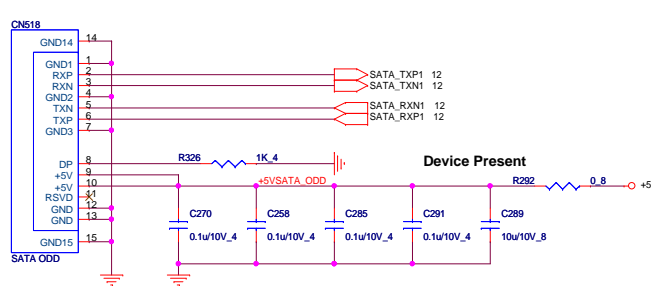


HDMI CEC

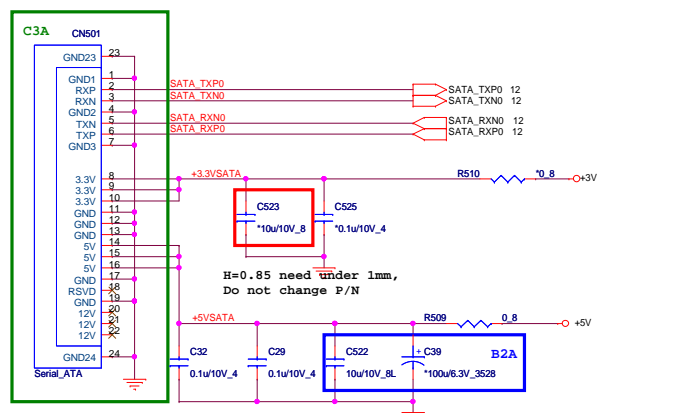


IV	USE	RN500, R400, R401, R134, R139, Q14, Q16
	DNI	RN2, R135, R140, R122, Q15, Q17, R127, R151, R128, R150
EV	USE	RN2, R135, R140, R122, Q15, Q17, R134, R139, Q14, Q16
	DNI	RN500, R400, R401, R127, R151, R128, R150

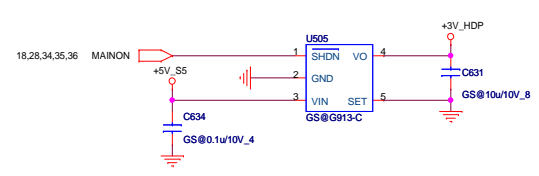
SATA ODD



SATA HDD



G SENSOR



FS (Full Scale) selection

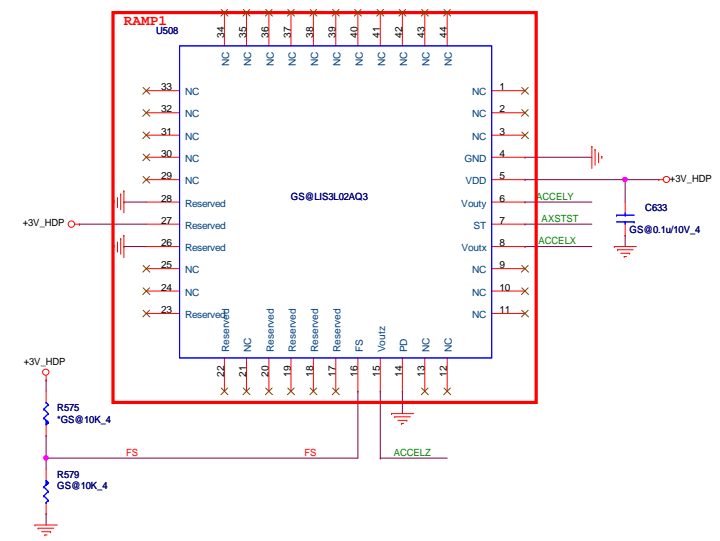
FS	0	1
	2g Full-Scale	6g Full-Scale

PD (Power Down) selection

PD	0	1
	Normal Mode	Power-down mode

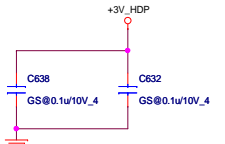
BOM Option Table

Reference	Description
GS@	G-SENSOR SEL

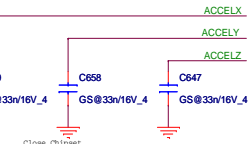
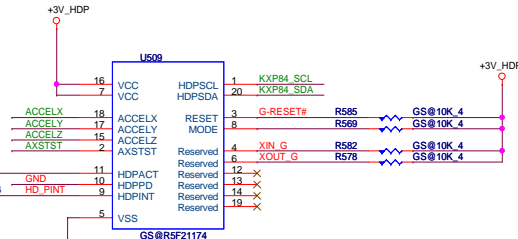


HDPPD selection

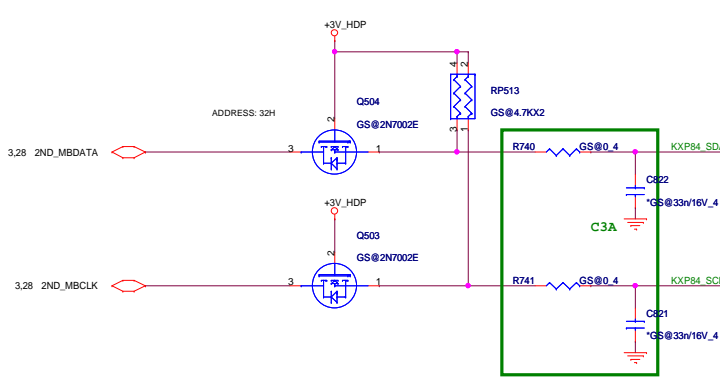
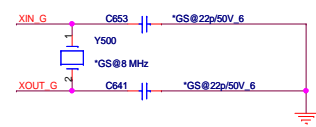
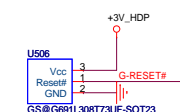
HDPPD	0	1
	Normal Mode	Power-down mode




Close to Pin 7 and Pin 16



Close chipset





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PROJECT : TELM

Size	Document Number	Rev
	HDD/ODD/G-SENSOR	E3D
Date: Monday, May 26, 2008	Sheet 22 of 40	

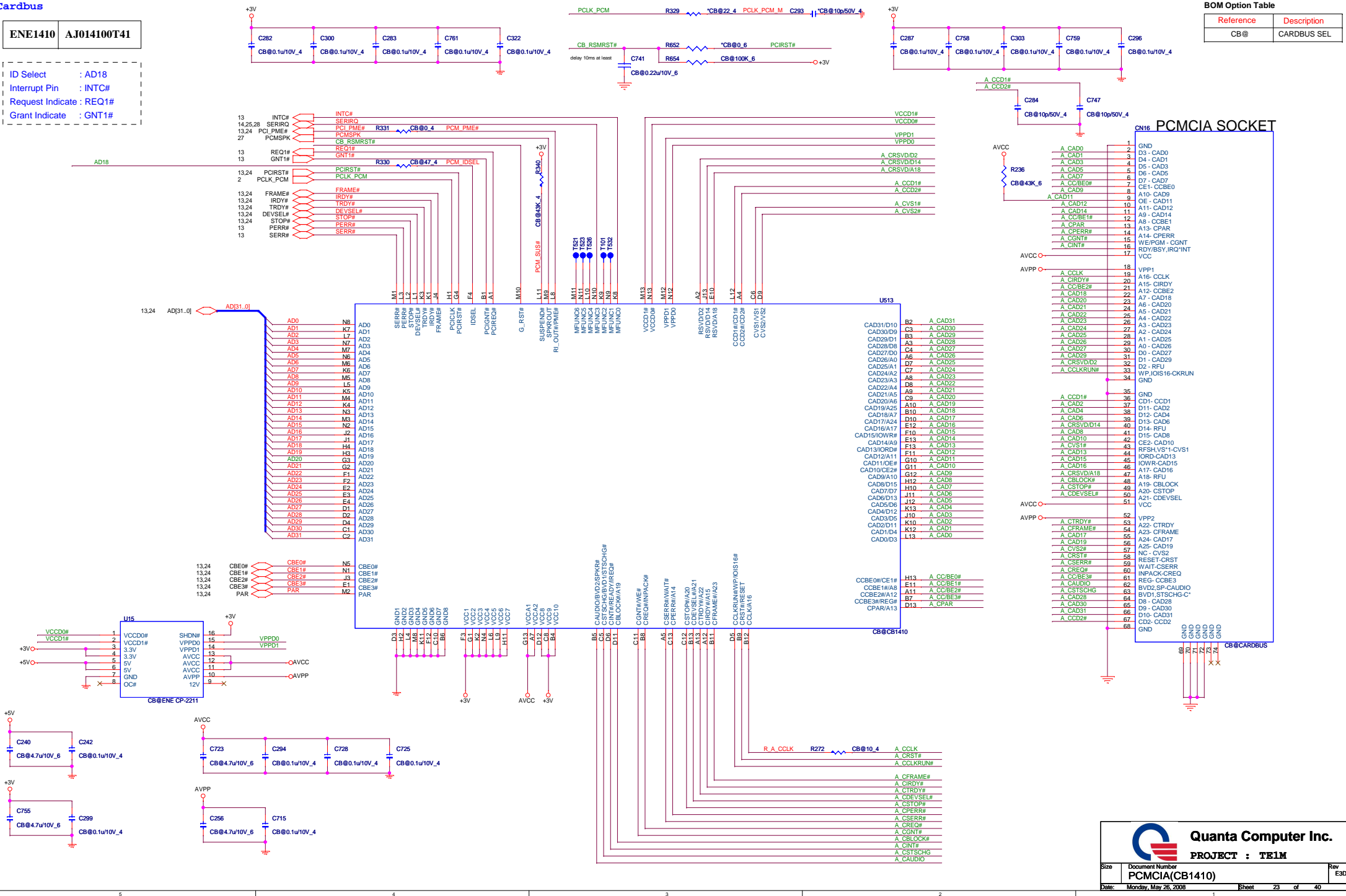
Cardbus

ENE1410	AJ014100T41
---------	-------------

ID Select : AD18
 Interrupt Pin : INTC#
 Request Indicate : REQ1#
 Grant Indicate : GNT1#

BOM Option Table

Reference	Description
CB@	CARDBUS SEL



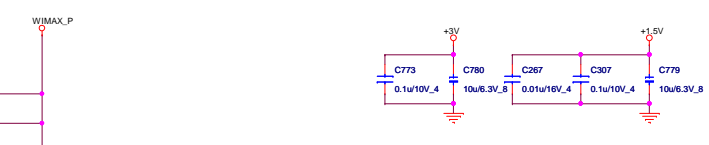
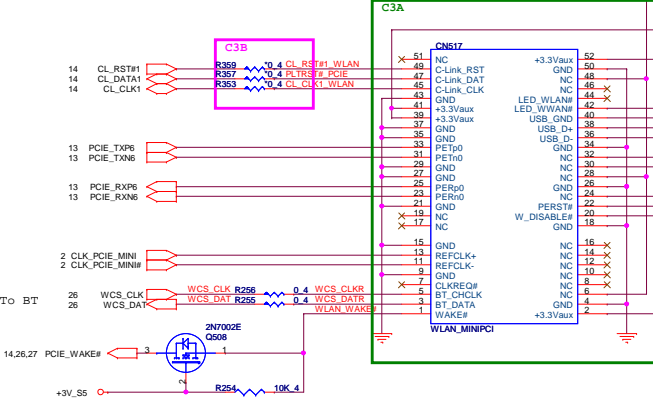
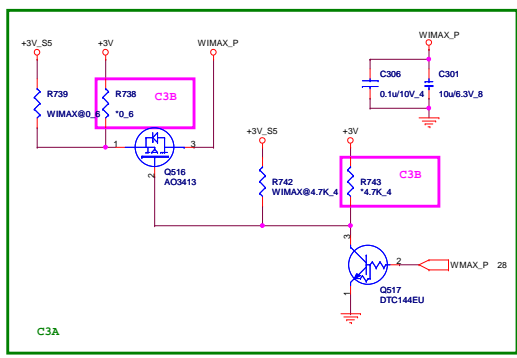
Quanta Computer Inc.
 PROJECT : TE1M

Size	Document Number	Rev
	PCMCIA(CB1410)	E3D

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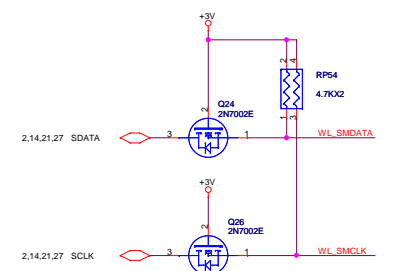
MINI Card 1 U&D 5.6H_WIMAX

1.5V_VDD(BOM) 0.5A
 3.3V_VDD(BOM) 1A
 3.3V_AUX(BOM) 0.005A



BOM Option Table

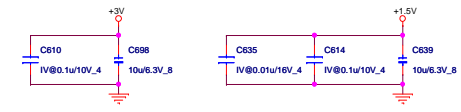
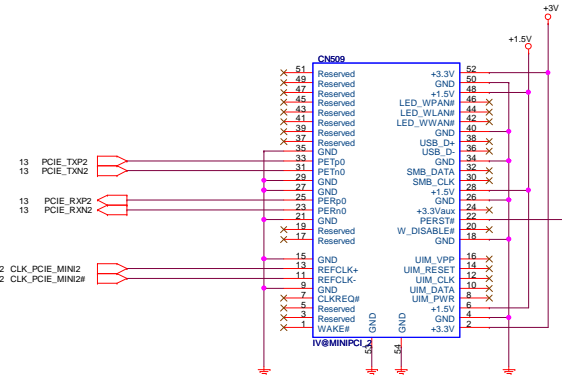
Reference	Description
IV@	INT VGA
EV@	EXT VGA
EV_IV@	EV&IV diff. BOM
WiFi@	WiFi Link
WIMAX@	WIMAX/WiFi Link



Pin	Signal	Value	Signal	Value
Pin 2,52	+3.3V		+3.3Vaux	
Pin 6,28,48	+1.5V		NC	
Pin 24	+3.3Vaux		NC	
Pin 39,40,41,42	NC		Pin 39,41 +3.3Vaux	
			Pin 40 USB_GND	
			Pin 42 LED_WMAN#	
Pin 46	LED_WMAN#		NC	
Pin 30,32	Pin 30 SMB_CLK		NC	
	Pin 32 SMB_DATA			

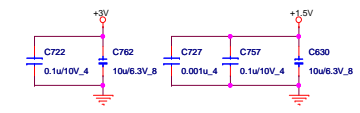
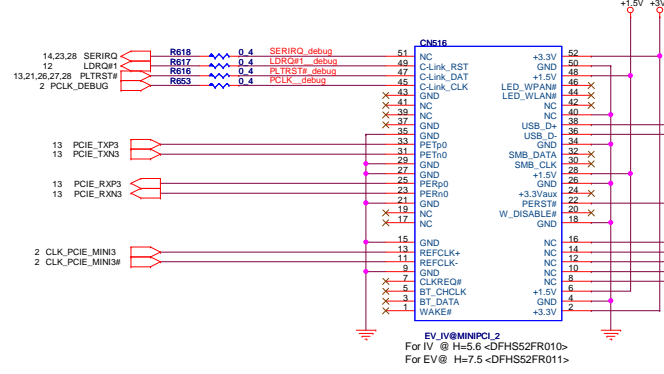
MINI Card 3 U 9H_HD-DVD

1.5V_VDD(BOM) 0.5A
 3.3V_VDD(BOM) 1A



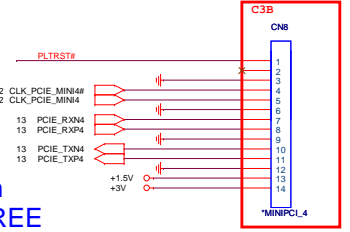
MINI Card 2 U 5.6H_TV/ROBOSON D 7.5H_HD-DVD

1.5V_VDD(BOM) 0.5A
 3.3V_VDD(BOM) 1A



EV_IV@MINIPCL2
 For IV @ H=5.6 <DFHSS2FR010>
 For EV @ H=7.5 <DFHSS2FR011>

MINI Card 4-D/Robson



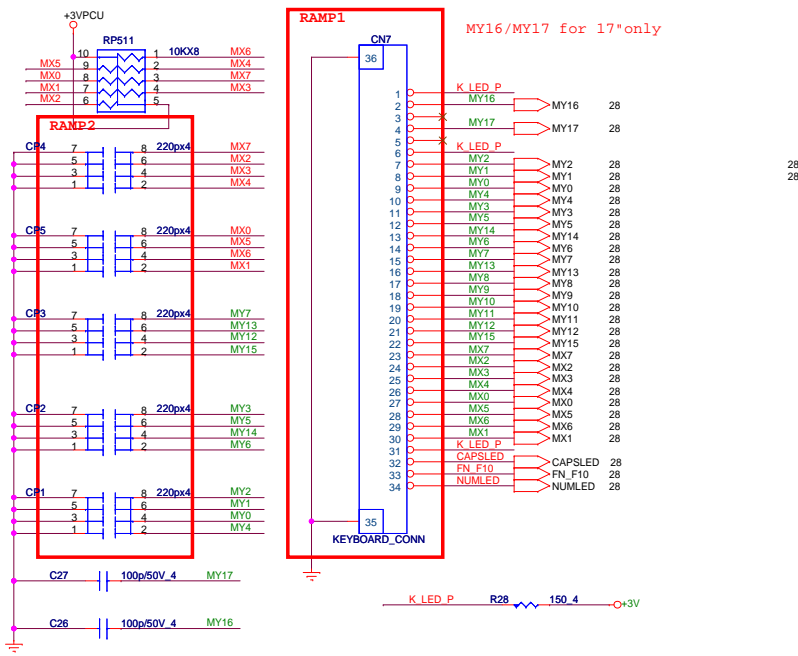
Remark1:TV/Robson or HD-DVD/Robson or TV-HD-DVD for DMA 800
 Remark2:TV is just for DMA(13*)

	UMA	Discrete
1	WLAN	WLAN
2	TV or Robson	HD-DVD
3	HD-DVD or Robson	N.C
4	N.C	Robson

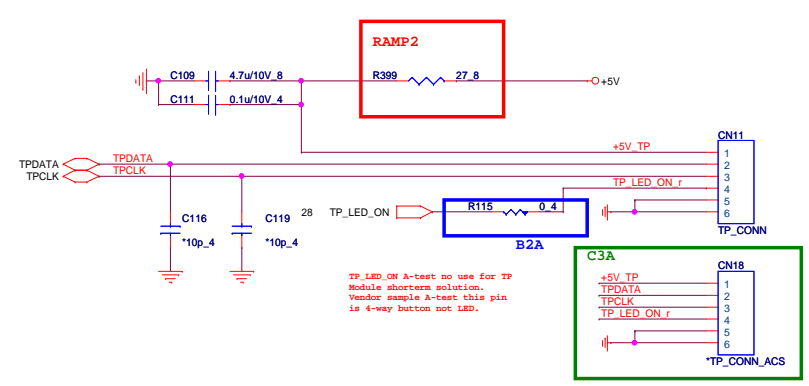
hexainf@hotmail.com
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 Size Document Number MINI CARD Rev ED
 Date: Monday, May 26, 2008 Sheet 25 of 40

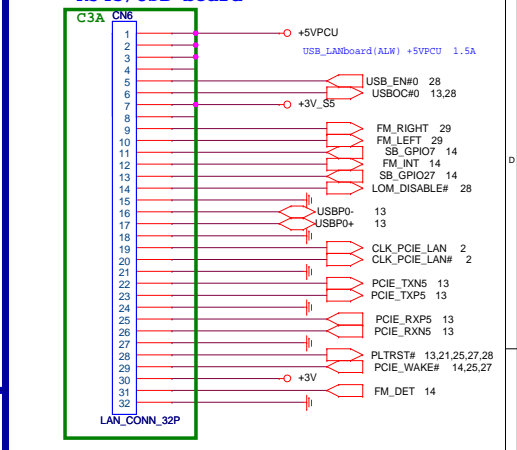
INT Keyboard



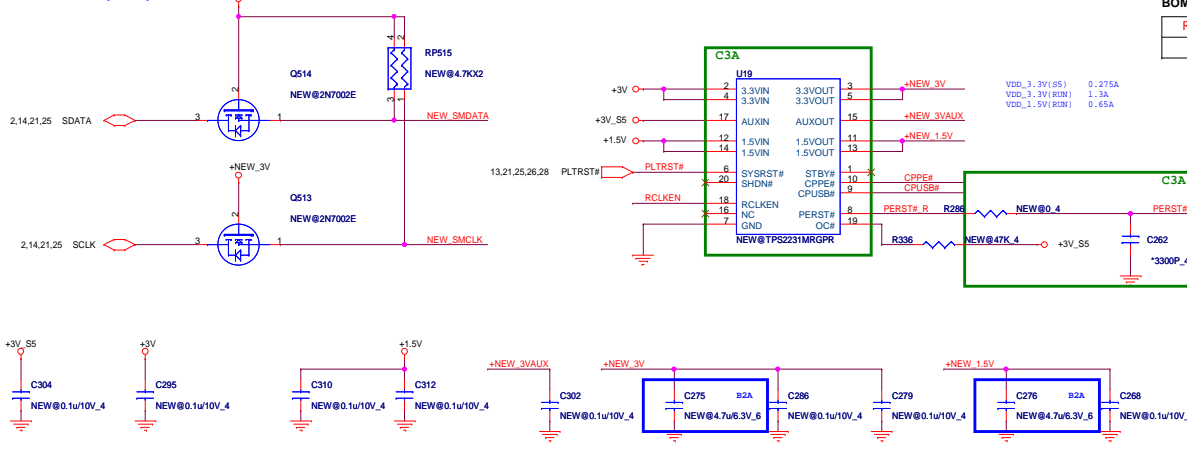
TP Board



RJ45/USB board

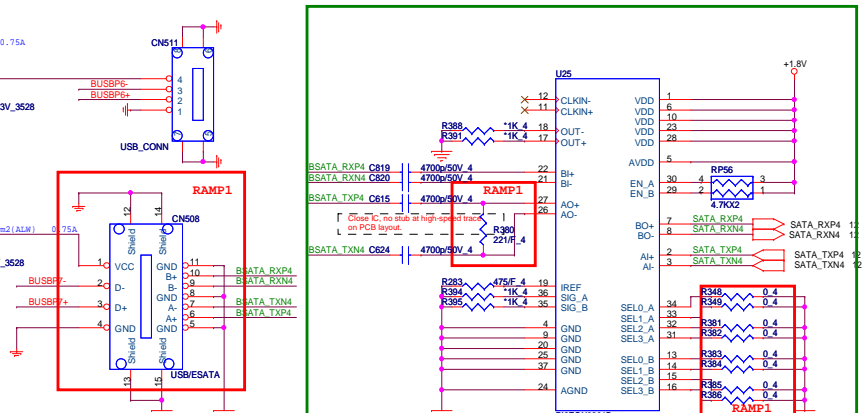
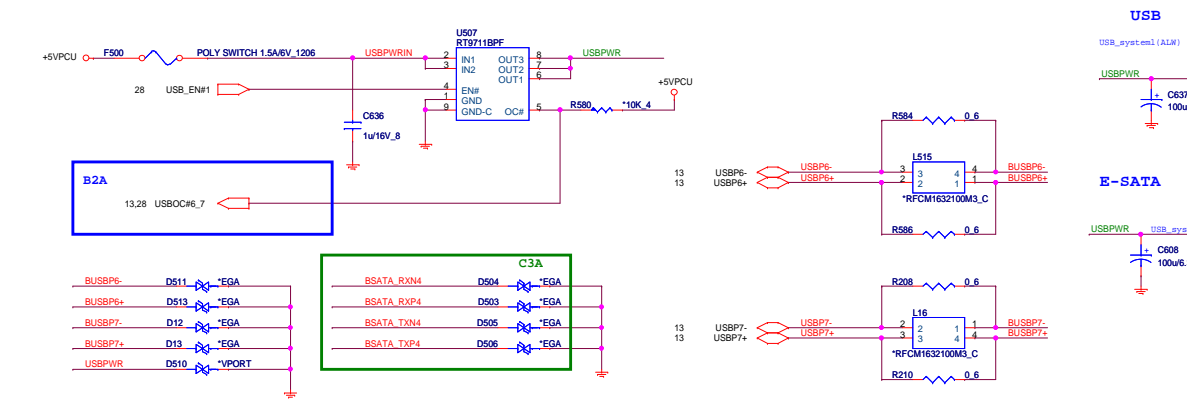
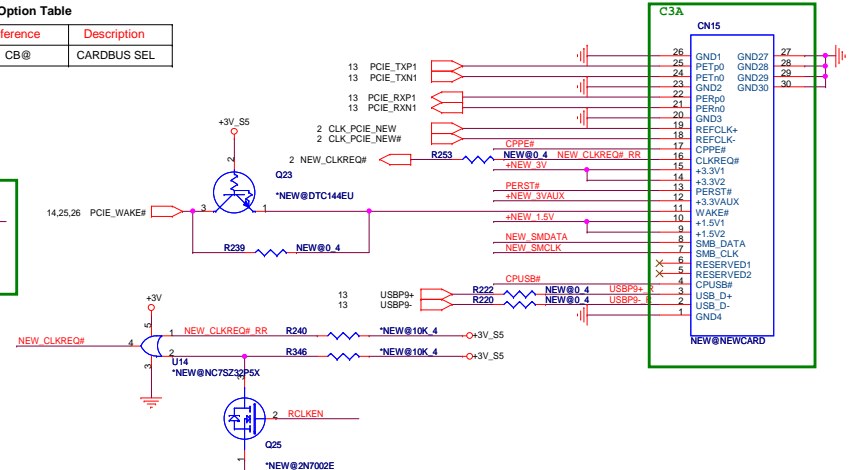


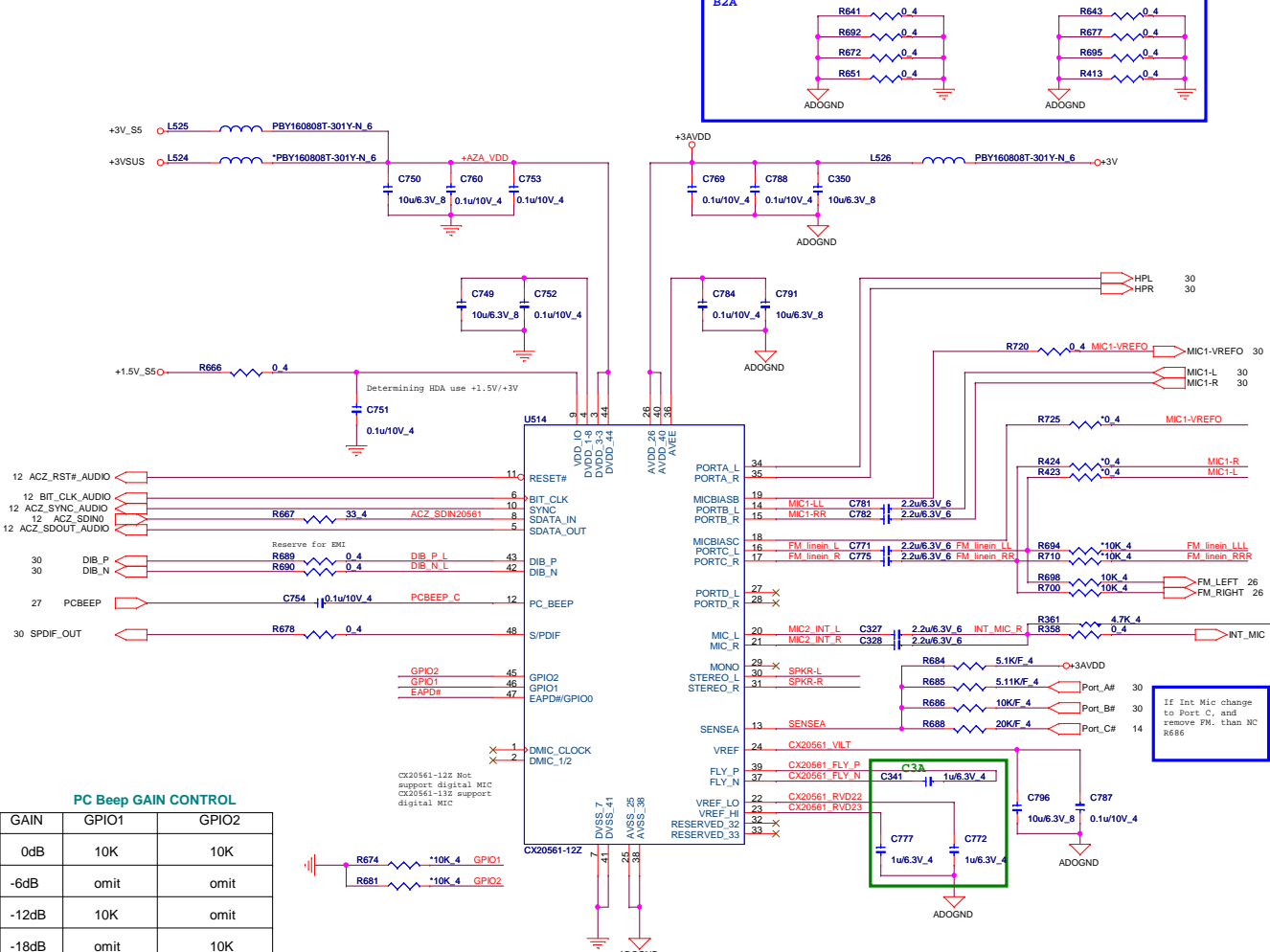
New card (BTO)



BOM Option Table

Reference	Description
CB@	CARDBUS SEL

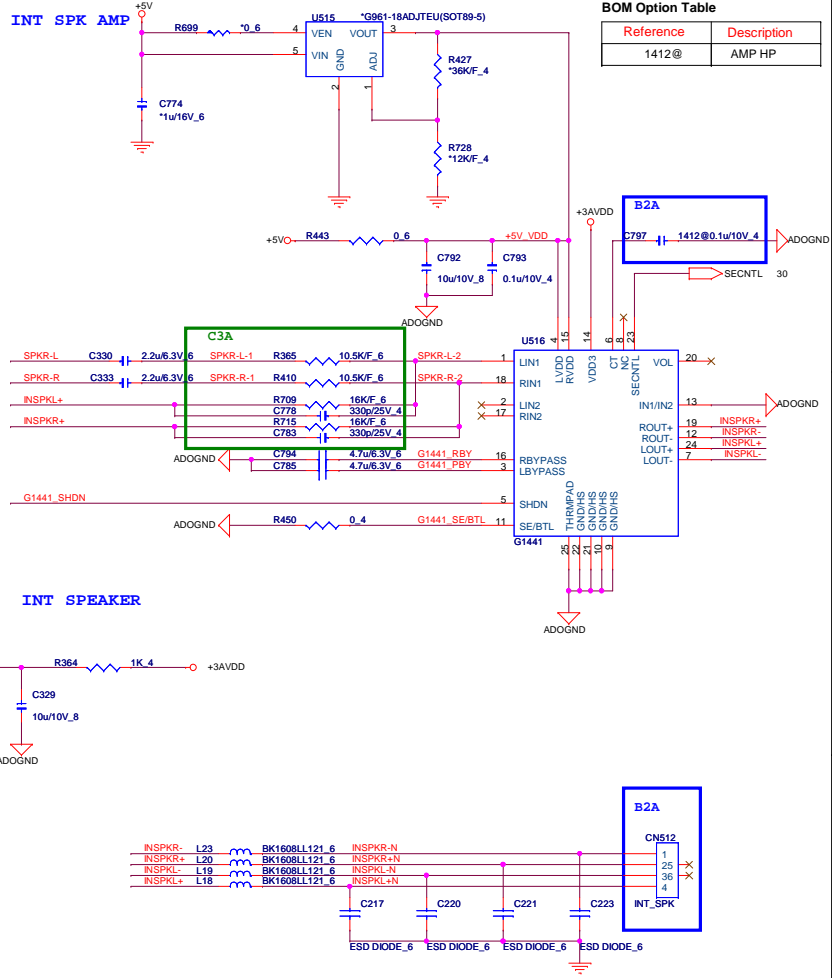
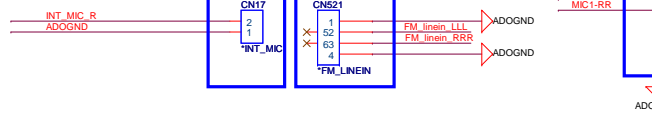




PC BEEP GAIN CONTROL

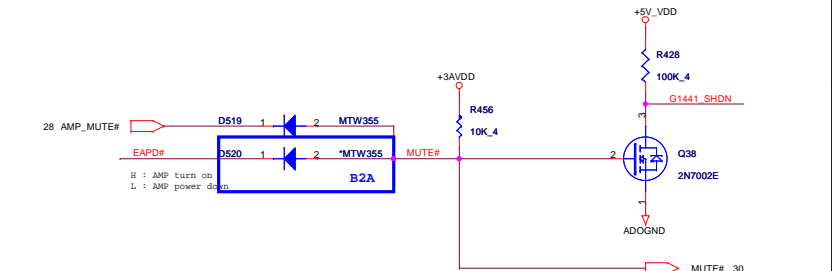
GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

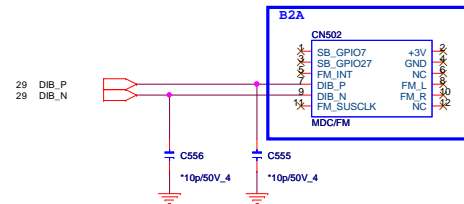
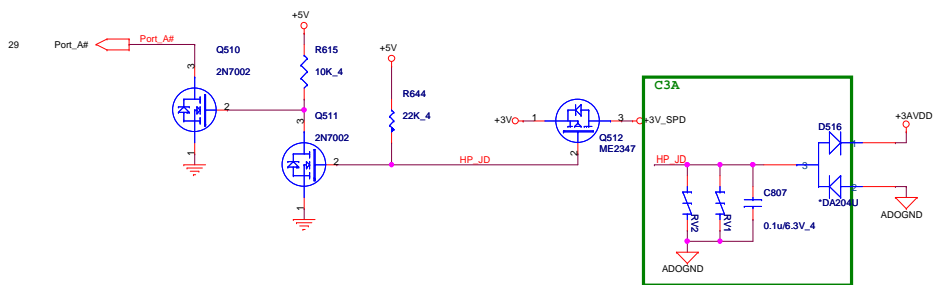
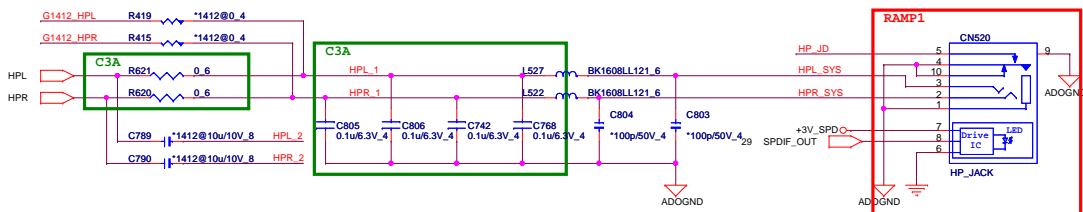
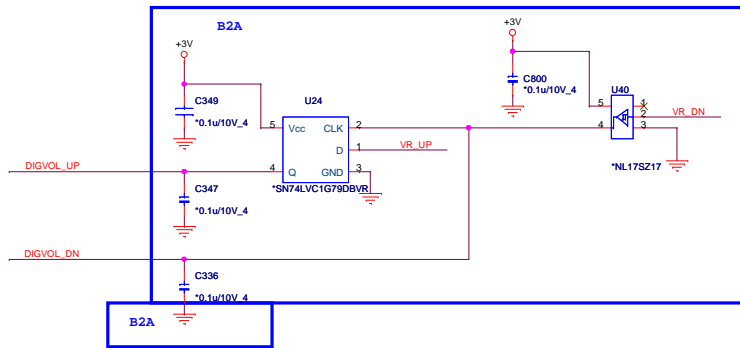
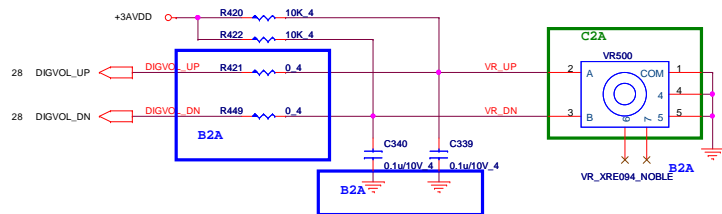
Reserve INTMIC



BOM Option Table

Reference	Description
1412@	AMP HP

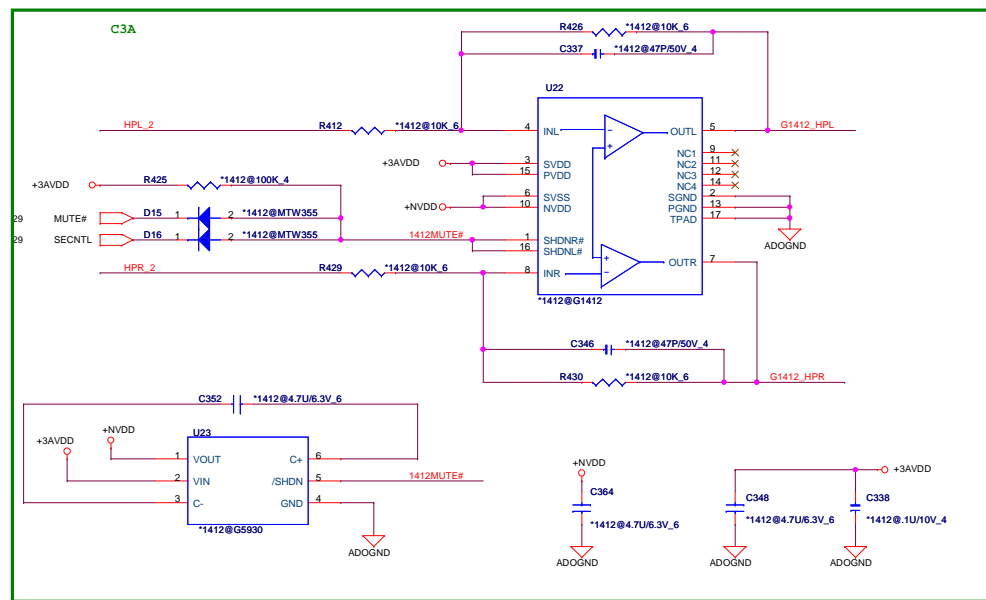
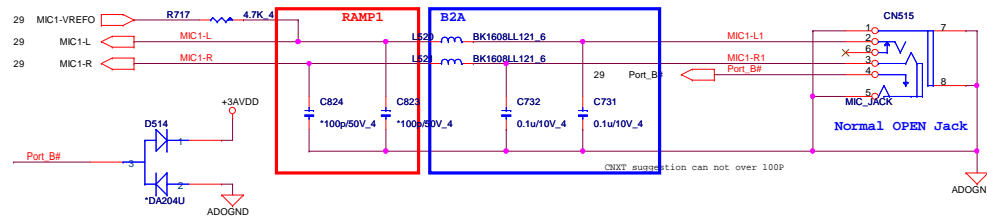


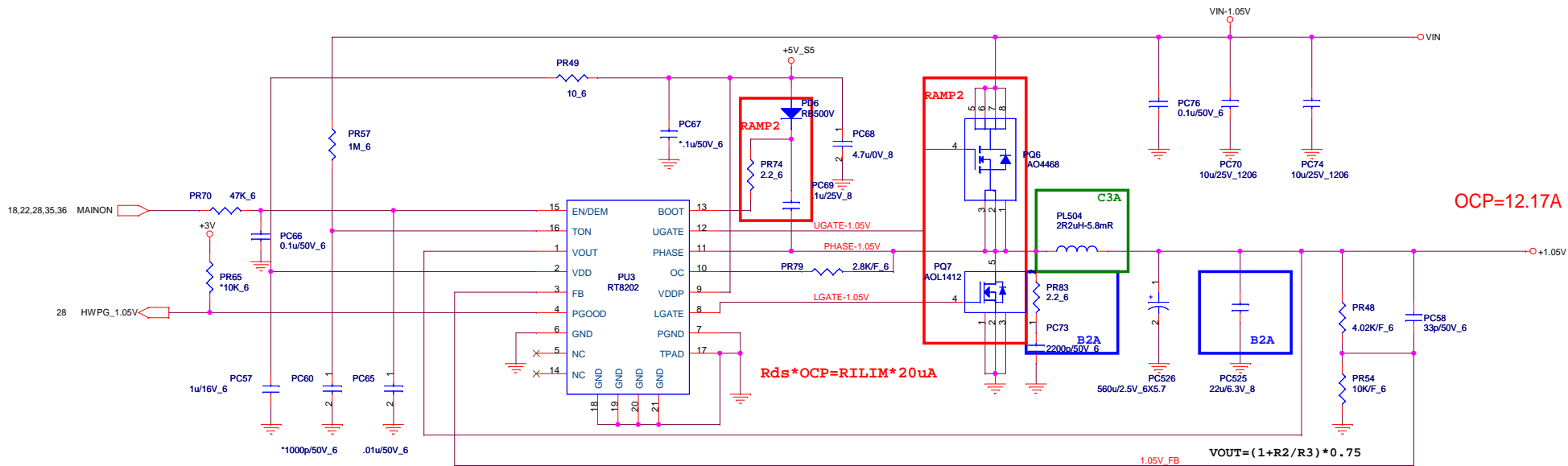


BOM Option Table

Reference	Description
1412@	AMP HP
CDCHP@	CODEC HP

TE1M REV:A Stuff both for test





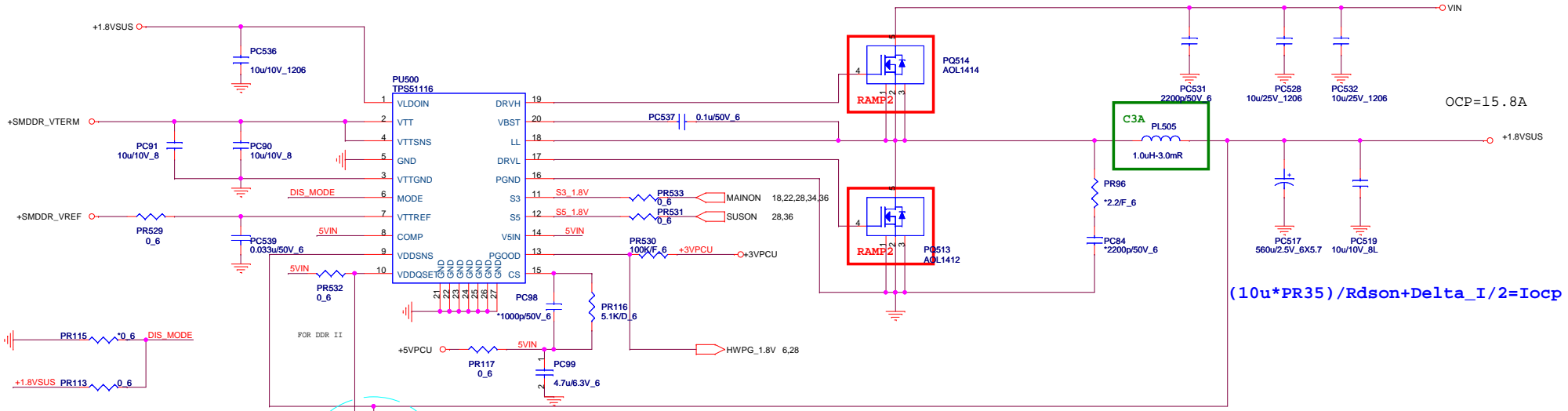
OCP=12.17A

$$TON = 3.85p * RTON * Vout / (Vin - 0.5)$$

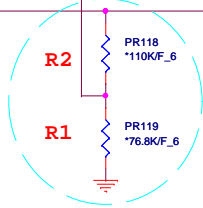
$$Frequency = Vout / (Vin * TON)$$

AO1412 Rds=4.6mOhm
12.17A OCP --- OC=2.8K (CS22803F914)

$$VOUT = (1 + R2/R3) * 0.75$$

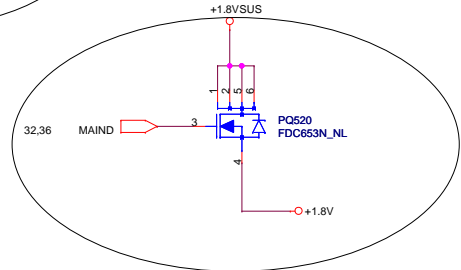
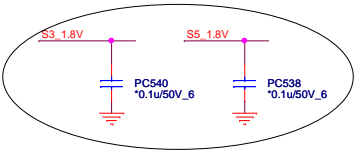


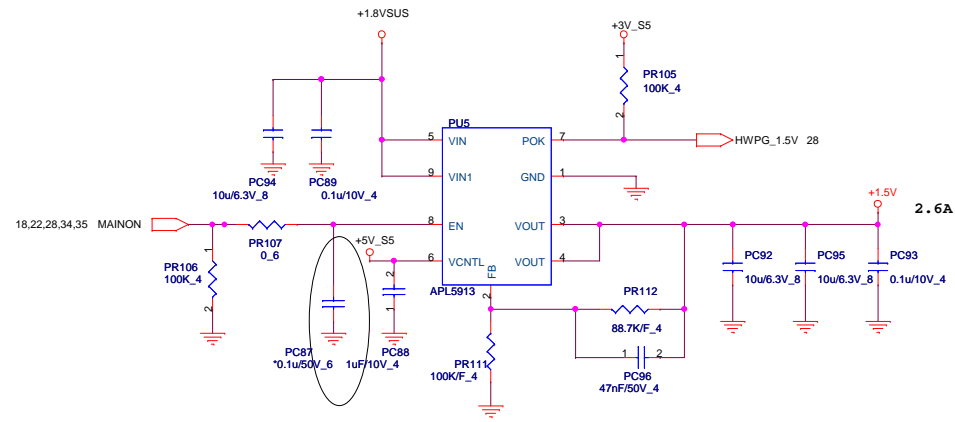
$$(10\mu * PR35) / R_{dson} + \Delta I / 2 = I_{ocp}$$



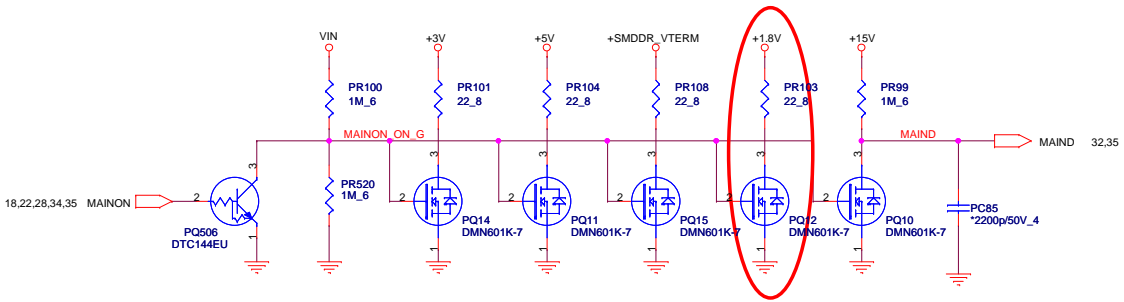
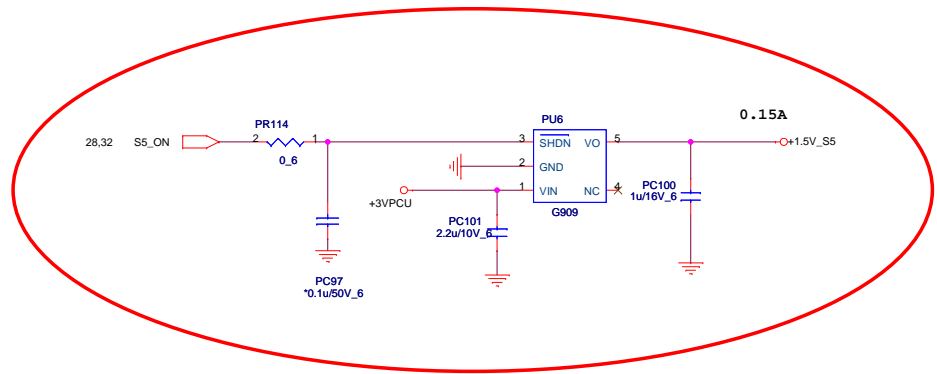
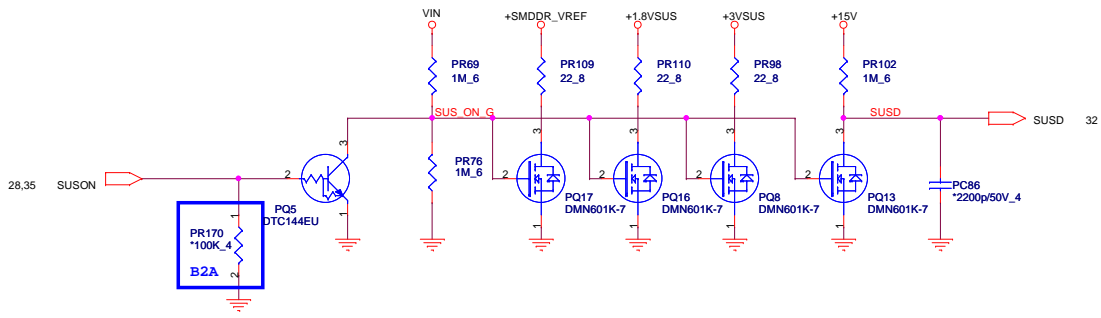
$$R1 = (100 * V_{out} - R2) / K$$

if tune Vout PR38 un-mount, PR156 PR165 mount

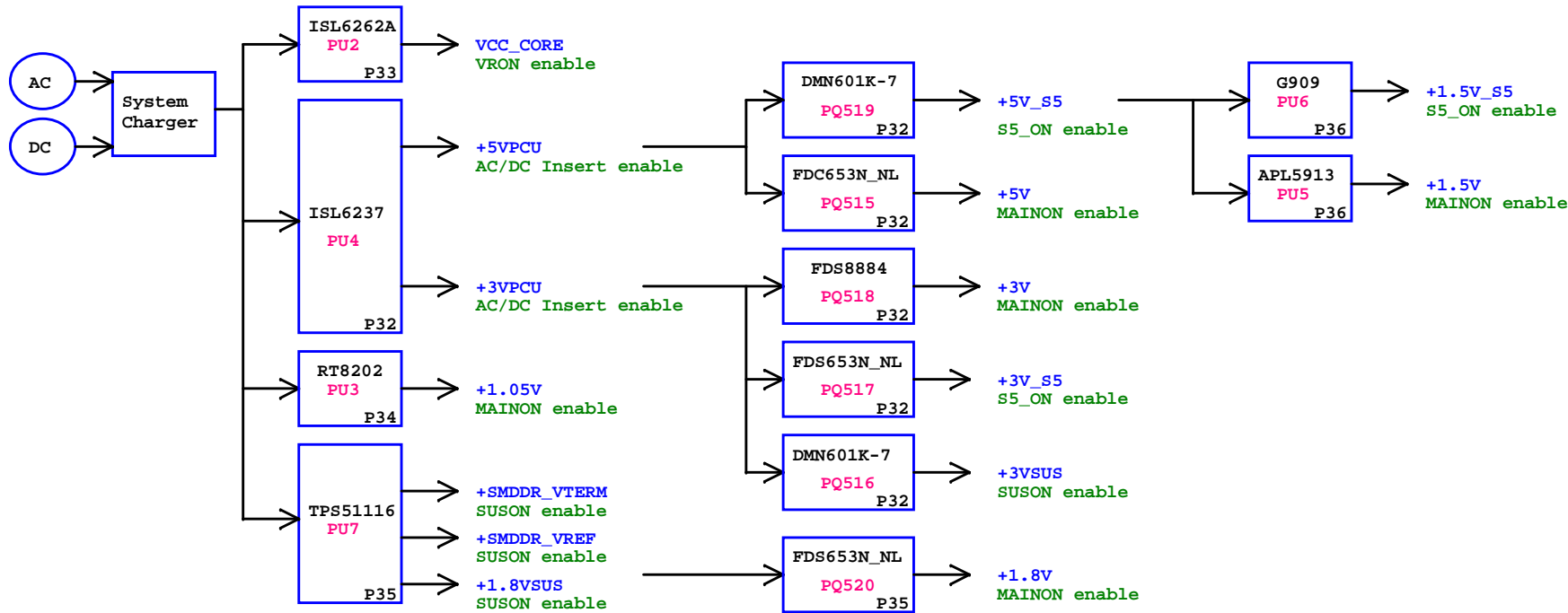




$$V_{out} = 0.8(1 + R1/R2) = 1.25V$$




Power Tree Table



Power Distribution List

Power	Distribution
VCC_CORE	CPU
+5VPCU	ICH9M, HDMI, MMB, Power Board, RJ45/USB Board, LED Board, USB, CIR
+3VPCU	ICH9M, HALL SENSOR, LCD/LED Panel, KB, MMB, Kill SW, EC, SPI Flash, CIR, ID
+1.5V	CPU, GMCH, ICH9M, Mini Card, New Card
+1.8VSUS	GMCH, DDR
+SMDDR_VREF	GMCH, DDR
+SMDDR_VTERM	DDR
+1.05V	CPU, CLK, Thermal Trip, GMCH, ICH9M
+5V_S5	ICH9M, G-SENSOR
+5V	CPU, ICH9M, VGA, Camera, CRT, HDMI, SATA HDD, SATA ODD, PCMCIA, TP/LED Board, Felica, WiMAX LED, EC, INT SPK AMP, HP
+3V	CLK, CPU Thermal Monitor, FAN, GMCH, DDR, ICH9M, VGA, LCD/LED Panel, HALL SENSOR, CRT, HDMI, SATA HDD, PCMCIA, Cardreader(OZ129T) Mini Card, KB, FP/LED Board, RJ45/USB Board, Bluetooth, New Card, PC Beep, EC, Codec(CX20561), HP, FM Tuner/MDC
+3V_S5	ICH9M, HDMI, Mini Card, RJ45/USB Board, New Card, Codec(CX20561)
+3VSUS	Codec(CX20561)
+1.8V	Cardreader(OZ129T)
+1.5V_S5	ICH9M, Codec(CX20561)


Quanta Computer Inc.
 PROJECT : TELM
 Size: Document Number
Power Tree Table
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